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(71) Applicant: O2 MICRO INTERNATIONAL LIMITED [—/—]; P.O. Box 32331 SMB, Grand Cayman (KY).

(71) Applicant and
(72) Inventor: LIN, Yung-Lin [US/US]; 2518 Indian Drive, Palo Alto, CA 94303 (US).

(72) Inventors: CHANG, Yu-Cheng; 904 Flying Fish Street, Foster City, CA 94404 (US). YAO, Bingwei; 801, Fuda 4-13-1, Chofu-Shi, Tokyo, Tokyo 182-0024 (JP).

(74) Agents: PFLEGER, Edmund, P. et al.; Grossman, Tucker, Perreault & Pfleger, PLLC, Suite 604, 795 Elm Street, Manchester, NH 03101 (US).

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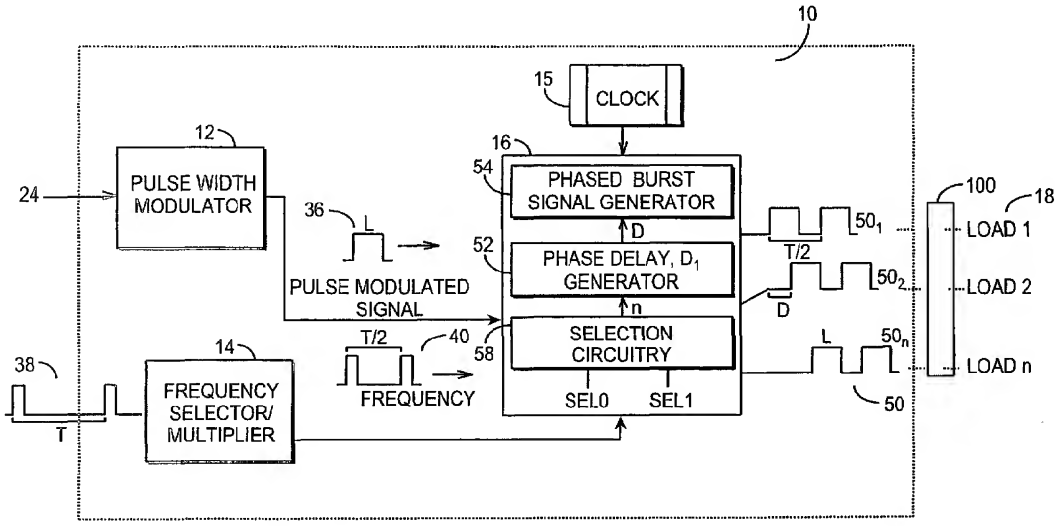

(57) Abstract: A sequential burst mode regulation system to deliver power to a plurality of loads. In the exemplary embodiments, the system (10) of the present invention generates a plurality of phased pulse width modulated signals (36) from a single pulse width modulated signal, where each of the phased signals regulates power to a respective load. Exemplary circuitry includes a PWM signal generator, and a phase delay array that receives a PWM signal (12) and generates a plurality of phases PWM signals which are used to regulate power to respective loads. A frequency selector circuit (14) can be provided that sets the frequency of the PWM signal (36) using a fixed or variable frequency reference signal.

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SEQUENTIAL BURST MODE ACTIVATION CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a sequential burst mode activation circuit. More particularly, the present invention provides a circuit topology, for improving the consistency of performance in the activation and intensity variation of multiple loads. The present invention has general utility wherever multiple loads are employed for intensity variation. Further, the present invention has specific utility where multiple fluorescent lamps, especially multiple cold cathode fluorescent lamps (CCFLs), are employed, for example, in television and computer screens, and in backlights for LCDs (Liquid Crystal Displays).

2. Description of Related Art

Various lighting and dimming circuits and techniques for lighting or dimming lamps or varying intensities of loads are known. One method of dimming a fluorescent lamp, especially as used in a backlight of a liquid crystal display (LCD), is known as a voltage controlled dimming system. The voltage controlled dimming system includes current control and current feedback control. According to the voltage control dimming system, dimming is performed by varying an input voltage to an inverter so as to adjust an output voltage from the inverter (i.e., an application voltage to the fluorescent tube). As the fluorescent tube emits light using discharging energy, when the application voltage to the fluorescent tube is too low, the discharging becomes unstable. For this reason, a large dimming range cannot be achieved by the voltage control dimming system, and the possible dimming ratio is only around 2:1, the dimming ratio being indicative of the dimming range of the lamp system.

Another technique for dimming a fluorescent lamp is the "burst mode" dimming system in which an alternating signal that is supplying power to the lamp is cut with a notch of variable width so as to reduce the power applied to the lamp and thereby provide the desired dimming. The smaller the widths of AC power provided to the lamp, the lower the luminance at which the lamp operates. A common device for providing the ability to vary the width of the pulses are commercially-available pulse-width modulators ("PWM").

In burst mode dimming, dimming is performed by periodically flashing the light source with a varying time ratio between the light-on duration and light-out duration. Therefore, this system, as opposed to the aforementioned voltage controlled dimming method, offers a large dimming ratio, potentially greater than 100:1, thereby allowing for large variations in luminosity.

U.S. Patent No. 5,844,540 provides lighting/dimming circuitry for the back light control function in an LCD (Liquid Crystal Display). A "PWM dimmer driving circuit" modulates the magnitude of current to be supplied through an inverter to a fluorescent tube on the back surface of a liquid crystal panel. One goal of this circuitry is to prevent inconsistency of lighting, or occurrence of flicker, between the back light, or fluorescent tube, and the LCD; the other goal is to reduce sound noise. The PWM and inverter circuitry modulates the light source driving means so as to have the ability to periodically flash the light source with varying time ratios between the light on and light off durations, thereby creating different average intensities of light. The light-on duration is determined by a 'pulse count circuit' which provides an input for the PWM circuitry; this pulse count circuit counts the number of pulses of the LCD panel horizontal synchronizing signal, and provides for an on-duration that allows for the back light to synchronize it's lighting signal with that of the LCD. Further, the lighting/on-off frequency of the light source is a division of the horizontal driving frequency of the LCD panel's horizontal synchronizing signal, thereby allowing both LCD panel's display and the back light to be in phase with each other. This topology provides a "burst-mode" dimming system but only for a single fluorescent lamp. It further advocates synchronization of backlight lighting with that of the LCD in order to prevent inconsistency of lighting between the LCD and backlight. Note that fluorescent lamps, especially cold cathode fluorescent lamps, are high in impedance when initially powered up. If multiple CCFLs (cold cathode fluorescent lamps) were utilized, synchronization of all lamps with one light source would result in current ripples; these current ripples retard inverter performance and cause flicker. This is because, where multiple CCFLs are synchronized, a power supply needs to provide enough power to turn on all CCFLs concurrently. The instant power delivered from the power supply causes the supply voltage to drop due to its limited dynamic response. Therefore, the use of PWM signals, i.e. "burst-mode"

dimming, is not, by itself, effective in providing a solution to flicker/noise in multiple lamp configurations.

One technique used to compensate for flicker or noise in the burst-mode dimming of multiple CCFLs is to place a capacitor in series with the power supply to absorb power surges that cause the current ripples. A drawback of this technique is that, when the lamps turn off in each burst mode cycle, the power supply line, which has an intrinsic inductance, continues to carry current which charges the capacitor, yielding an increase in output voltage.

Prior art teachings with the activation with multiple loads, where the loads are not fluorescent lamps, do not address the flicker or noise problem presented by the activation of multiple lamps.

SUMMARY OF THE INVENTION

Accordingly, the present invention solves the drawbacks of the prior art by providing a sequential burst mode activation circuit for multiple loads by generating a phase shift between multiple burst-mode signals. The burst mode signals are used to regulate power delivered to loads, where each load is regulated by a separate phase-shifted burst signal such that at least two loads do not turn on synchronously. The circuit of the present invention overcomes prior art regulation circuits by eliminating instantaneous high current ripples and noise created by multiple loads turning on simultaneously.

The present invention provides a sequential burst mode activation circuit comprising a variable power regulator, comprising a pulse modulator generating a pulse signal having a pulse width; a frequency selector generating a frequency selection signal; and a phase delay array receiving said pulse signal and said frequency selection signal, and generating a plurality of phased burst signals, wherein at least two of said phased burst signals have different start times.

In method form, the present invention provides a method for generating phase shifted burst mode signals, comprising the steps of generating a pulse signal having a pulse width, generating a frequency selection signal, generating a plurality of phased burst signals having a frequency of said frequency selection signal and pulse width of said pulse signal, and delaying at least one of the phased burst signals to have a different start time than at least one other of the phased burst signals.

The present invention also provides a phased burst mode dimming system, comprising: a pulse width modulator generating a pulse width modulated signal; a variable selector for selecting the width of said pulse width modulated signal; and a phase delay array receiving said pulse modulated signal and said frequency selection signal, and generating a plurality of phased burst signals by generating a phase delay between at least two said pulse width modulated signals.

In one exemplary embodiment, power is regulated to a plurality of loads using the plurality of phased burst signals. Additionally, a constant or variable phase delays is generated between each phased burst mode signal. In an exemplary system, the present invention provides a sequential burst mode dimming circuit for multiple lamps. In particular, the exemplary system provides a sequential burst mode dimming circuit for a plurality of cold cathode fluorescent lamps (CCFLs). Customer or software inputs vary the pulse width of a PWM signal, thereby determining the power to be delivered to the lamps. A reference signal is doubled to select the frequency of the PWM signal. This selected frequency determines the frequency at which lamps turn on and off. Using a counter and a clock, multiple phased burst signals are generated from the above burst signal for the plurality of CCFL's. Each phased burst signal is shifted by a constant phase shift such that at least two lamps receive burst signals that are out of phase. Therefore, sequential burst-mode activation of each lamp is generated. Finally, in the exemplary system, a plurality of phase array drivers, each of which uses feedback from a corresponding lamp in combination with a corresponding phased burst signal, delivers power to and regulates the intensities of a corresponding plurality of lamps.

Another exemplary system of the present invention includes a frequency selector that generates a frequency selection signal for a backlight load which follows, as reference, a conventional screen updating frequency of a cathode ray tube (CRT) in a television set. In yet another exemplary system, a phase delay array generates a plurality of phased burst signals, such that no two phased burst signals have different start times. In an example of such an embodiment, a phase delay array generates a constant or variable phase delay so that each of the phased burst signals is delayed by such a phase delay from another of the phased burst signals.

It will be appreciated by those skilled in the art that although the following Detailed Description will proceed with reference being made to exemplary systems and methods of use, the present invention is not intended to be limited to these exemplary systems and methods of use. Rather, the present invention is of broad scope and is intended to be limited as only set forth in the accompanying claims.

Other features and advantages of the present invention will become apparent as the following Detailed Description proceeds, and upon reference to the Drawings, wherein like numerals depict like parts, and wherein:

Brief Description of the Drawings

Figure 1 is a top-level block diagram of an exemplary sequential burst mode signal generation system of the present invention;

Figure 2 is a more detailed block diagram of the exemplary sequential burst mode signal generation system of the present invention;

Figure 3 is a signal representation of the pulse width modulator of the exemplary sequential burst mode signal generation system of the present invention;

Figure 4 is a signal representation of the phase delay array of the exemplary sequential burst mode signal generation system of the present invention;

Figures 5(a) and 5(b) are charts of 'select' signal inputs to circuitry reflecting the resulting number of loads;

Figure 6 provides a summary of the signals discussed in Figure 1 through Figure 5;

Figure 7 is an exemplary IC implementation of the sequential burst mode generation system of the present invention;

Figure 8 is a top level diagram of phase array drivers of the present invention;

Figure 9 is a circuit example showing how a phase array driver generates a power regulating signal in the present invention;

Figure 9a is a signal diagram of the load current;

Figure 10 is a timing diagram showing how a phase array driver generates a power regulating signal in the present invention;

Figure 11 is a power regulating signal generated by an exemplary phase array driver of the present invention;

Figure 12 is an exemplary IC implementation of a phase array driver IC in the present invention;

Figure 13 is a circuit example showing how a phase array driver generates a voltage clamping signal in an exemplary IC of the present invention;

Figure 14(a) and 14(b) provide circuit examples of half-bridge and full-bridge (H-bridge) topologies respectively;

Figure 15 provides a signal generation example showing the generation of cross switch signals in a full-bridge topology.

Detailed Description of the Exemplary Embodiments

The following description will reference a burst mode regulating circuit for a plurality of cold cathode fluorescent lamps (CCFLs). CCFLs are arranged, for example, in large panels for displays. Typically, large CCFL panels each utilize a minimum of 6 lamps, and the present invention will describe a burst mode activation circuit with 6 or more CCFls. Of course, the present invention is not to be limited by a minimum number of loads, nor is it to be limited to CCFLs or any particular type of loads.

Figure 1 is a top-level block diagram of an exemplary sequential burst mode signal generation system 10 of the present invention. As a general overview, the sequential burst mode signal generation system 10 operates to generate phase-shifted burst mode signals 50 and sends these burst mode signals to drivers 100 to provide time-delayed regulation of power to a plurality of loads 18. "Burst mode", as used herein and as is understood in the art, generally means regulation of power to a load using a PWM signal to modulate the power delivered to the load based on the pulse width of the PWM signal. System 10 generally includes modulator 12 generating a pulse modulated signal 36, frequency selector 14 generating a frequency selection signal 40 for setting the frequency of the pulse modulated signal, and phase delay array 16 generating multiple phase-shifted burst signals 50. Advantageously, by independently regulating a plurality of loads 18 with a plurality of phase-shifted burst signals 50, thereby substituting the need for a single high power input with the adequacy of multiple low power inputs, the system 10 of the present invention resolves the aforementioned problems with conventional multiple load power regulation circuit.

Figure 2 is a more detailed block diagram of the system 10 of the present invention. Pulse modulator 12 generates a PWM (pulse width modulated) signal 36 having a pulse width L, whose duty cycle (i.e. pulse width) determines power delivered to a load 18. The frequency selector 14 selects the frequency of the PWM signal 36, based on an independent reference signal 38 of period, T. In an exemplary embodiment, for reasons that will become apparent below, frequency selector 14 comprises a multiplier to multiply the frequency of the reference signal 38 (of period, T) by a factor of k, and generate a multiple signal 40 (of period, T/k), where the multiple signal 40 is used to set the frequency of the PWM signal 36. For example, where the system 10 is utilized to regulate multiple CCFLs, a synchronizing signal, or Vsync, may be used as the reference signal 38. In an example where CCFLs are utilized in television, video, or LCD screens, Vsync 38 is an available video signal used to update the on-screen display. The use of Vsynch may be desirable since if an arbitrary reference signal is selected independently of screen updating frequency then a "beat" may occur. A "beat" is understood by one skilled in the art to manifest itself in the following manner. A video display is transmitted across a television monitor by a cathode ray tube (CRT). The CRT, upon completing transmission of a display, returns to a starting position and proceeds to transmit the next display. The displays are refreshed at a frequency defined by Vsync. In the duration between the completion of one display transmission and the initiation of the next, no information is broadcast and the television screen is kept dark. If light is introduced in this duration, the transition of the CRT to its starting position may reveal visual lines superposing different displays. This is known in the art as 'beat.' If the frequency of burst mode regulation of lamps were not to follow Vsync frequency, light would be introduced during the aforementioned duration, thereby allowing for beats. Further, the screen updating frequency is multiplied because if a CCFL frequency is equal to and not a multiple of the screen updating frequency, the concurrent intensities of light may result in flicker. Thus, Vsync is a desired reference signal for the above exemplary applications.

In the exemplary embodiment where the reference signal 38 is multiplied to generate the multiple signal 40, it should be noted that when period T/k (k is the multiplier of signal 38) of the multiple signal 40 is greater than L of signal 36, that is,

when period T of signal 38 is greater than k*L, each burst signal 50 will comprise distinct pulses. If the period T is equal to or less than k*L, then each burst signal 50 would be a high DC signal (i.e., each burst signal 50 would represent a full power setting). This is discussed further below. In the example in Figure 2, frequency selector 14 doubles the frequency (i.e., k=2) of independent reference signal Vsync 38, thereby generating a frequency selection signal 40 having period of T/2. Both signal 36 and 40 are input into phase delay array 16 to generate a plurality of phased burst signals 50, as described below.

Phase delay array 16 includes phase delay generator 52 to determine a phase delay value, D, between successive phased burst signals, 50_1, 50_2,...50_n; load selection circuitry to determine the number of loads n; and circuitry 54 to generate multiple phase-delayed pulse width modulated signals 50_n. Each of these components is described in detail below.

Referring briefly to Figures 5(a) and 5(b), depicted are charts of 'select' signal inputs to selection circuitry 58. These inputs are used to quantify the number n of loads 18 coupled to circuit 10 of the present invention. Note that n also quantifies the number of phased burst signals 50. In an exemplary embodiment, selection circuitry 58 operates as a state machine to generate an appropriate signal to the phase delay generator 52 based on the binary value of input "select" signals. Figure 5(a) illustrates "select" signal generation of an exemplary embodiment, where a minimum of 6 CCFLs are utilized. This table includes two inputs: Sel0 and Sel1, each generating a binary value indicative of the number of CCFLs. In this table, 6 CCFLs are represented by Sel0=0 and Sel1=0. Further CCFLs (added by increments of two) are defined in this table. The table of Figure 5 (b) generalizes the above example of Figure 5(a) to include less than a minimum of 6 and more than a maximum of 12 CCFLs. Generally, more select signal inputs 58 allow for a greater number of loads 18 to be utilized, i.e. a larger n. In this example, an additional select input is provided: Sel2, permitting additional loads to be defined. For reasons that will become apparent below, in the example using CCFLs as loads, it is desirable to define an even number of lamps in the circuit. Of course, those skilled in the art will recognize that the tables of Figures 5(a) and 5(b) and the selection circuitry 58 could be adapted to define any number of loads.

Figure 3 provides a signal representation of the pulse width modulator 12. Pulse width modulator 12 generates a pulse width modulated signal 36 whose pulse width, L, is set by variable selector 24. Variable selector 24 is provided to permit variable power (i.e. dimming) to be delivered to the load by changing the pulse width, L, of the PWM signal. Variable selector 24 varies the value of a DC signal 30 proportional to a desired dim setting. In an exemplary embodiment, the variable selector 24 comprises a dim selector 26 and a polarity selector 28. The dim selector 26 determines the desired dim setting by increasing or decreasing a DC signal 30. The polarity selector 28 is discussed further below. Oscillator 22 generates a triangular waveform 34 of predetermined frequency as an input to the pulse width modulator 12. The DC signal 30 is superimposed upon the triangular waveform 34. In one exemplary embodiment, illustrated in Figure 3, a section, defined by the intersections of the DC voltage 30 with each of the rise, 25a, and fall, 25b, of each triangular wave 34, determines the leading and falling edges of each pulse, and thereby the pulse width, L, of a pulse width modulated signal 36. In this embodiment, a higher value of DC signal 30 generates a smaller pulse width, L and a lower value of DC signal 30 generates a larger pulse width, L. In an alternative embodiment, a section defined by each falling edge, 25b, and the next rising edge, 25c, is used to generate the pulse width, L. In this alternative embodiment, a higher value of DC signal 30 generates a larger pulse width, L, and a lower value of DC signal 30 generates a smaller pulse width, L. The polarity selector 28 determines which section of the intersections of the DC signal 30 and triangular waveform 34 is used to generate the pulse width, L. Thereby, the pulse width modulator 12 generates a PWM signal 36 of pulse width, L, determined by the user selection 24.

Figure 4 is a detailed block diagram and signal representation of phase delay array 16. Phase delay array 16 determines a phase delay value, D, and generates phased burst signals 50, as a function of L, T/2 and the number n. Phase delay array 16 receives as inputs a clock signal 15, PWM signal 36 having pulse width L, select signal inputs 58, and a reference signal 40 of doubled frequency, i.e., having a period of T/2. Preferably, the value of D is determined such that the phase shift between each phased burst signal 50 is constant, i.e. D is constant. Further, the phase delay D repeats itself between the last phased burst signal and the first, i.e., where there are n

phased burst signals 50, each pulse, p, of phased burst signal n, 50_n, is preferably leading by phase shift, D, from the next pulse, p+1, of phased burst signal 1, 50_1. To accommodate this in the preferred embodiment, phase delay D equals (T/2)/n where T is the period of reference signal 38, T/2 is the period of signal 40, n is the number of phased burst signals 50, and the frequency of each phased signal 50 is equal to the frequency of signal 40. Those skilled in the art will recognize that, alternatively, the present invention may include variable phase delays such that the phase delay value is not constant but that some or all of the loads 18 still turn on at different times. Such alternative embodiments are included in the scope of the present invention.

In an exemplary embodiment, circuitry 54 includes a counter 56 with a clock input 15 to generate n phased burst signals 50 given the aforementioned inputs. Specifically, a counter 56 may be implemented with a series of toggling flip-flops wherein a clock pulse at a time of t triggers the first pulse of a first phased burst signal 50_1, while a clock pulse at a time of t+D triggers the first pulse, p, of a second phased burst signal 50_2. Likewise, the clock pulse at a time of t+2D triggers the first pulse of a third phased burst signal 50_3 and a clock pulse at a time of t+(n-1)*D triggers the first pulse of an nth phased burst signal 50_n. Thereupon, the clock pulse at t+(n)*D, triggers the second pulse of the first phased burst signal 50_1. Since the period of each signal is T/2 where T is the period of the independent signal 38, it follows that [(t+nD) – t] equals T/2. In other words, n*D equals T/2, or D equals (T/2)/n.

Further, each phased burst signal 50 has pulse width, L. To accommodate this, the first pulse of an mth phased burst signal 50_m, where 1 m n, is generated by sampling the clock signals starting at clock signal, t + (m-1)D, for a duration dictated by variable pulse width L. Subsequent phased burst signals 50 follow the same paradigm. Therefore, the first pulse of the first phased burst signal 50 may be generated from clock pulses, t, t+1, t+2, ..., t+(L-1), such that L clock pulses account compose the pulse width L of each phased burst signal pulse, p. As noted earlier, to generate distinct pulses for each phased burst signal 50, L should be less than T/2. That is, if L is not less than T/2, each phased burst signal 50 will be a DC signal with no distinguishable pulses.

Figure 6 summarizes signals discussed in Figures 1-5 above for an exemplary embodiment. Signal 34 is the triangular waveform generated by the oscillator 22

(Figure 3). DC signal 30 is superimposed onto signal 34, and shifted up or down, i.e., increased or decreased, to produce a desired dimming. The intersections of signal 34 with DC signal 30 determine the rising and falling edge of each pulse of the pulse width modulated signal 36, thereby determining the pulse width, L, of each pulse of the pulse width modulated signal 36. Signal 36 follows the frequency of signal 34. The pulse width, L, of signal 36 is utilized to generate phased burst signals 50 (i.e., 50_1 to 50_n), while the frequency of signal 36 is not. The frequency of phased burst signals 50 is determined by an independent reference signal, Vsync 38, of period T. Vsync 38 is doubled to generate signal 40 of period T/2, i.e., frequency 2/T. The phased burst signals 50 are timed by this frequency, 2/T. The number of phased burst signals 50 is determined by an input as to the number of loads to be utilized. In the example, six (6) loads are utilized. Therefore, six (6) phased burst signals 50 are displayed, where each phased burst signal, for e.g., 50_2, lags the previous phased burst signal, for e.g., 50_1, by (T/2)/6 = T/12.

Figure 7 is an exemplary IC (integrated circuit) implementation 60 of the sequential burst mode signal generation system 10 of the present invention. The IC 60 comprises a PWM generator 12, Vsync detector & phase shift detector 13, frequency multiplier 14, and a phase delay array 16. Components 12, 14 and 16 are described above with reference to Figures 1-5. The exemplary IC 60 also includes a clock 15, an oscillator 22 to generate the triangular waveform 34, buffers 19 to amplify the current driving capacity of phased burst signals, and under voltage lockout protection circuitry 2.

The PWM generator 12 receives DIM, polarity, LCT, and a clock (100KHz Generator) signal as inputs. The PWM generator 12 generates a PWM signal 36 as discussed above. Further, as described above, the pulse width of the PWM signal generated by generator 12 is selected using the DIM and polarity inputs. LCT of the exemplary IC 60 is the oscillator 22 input generating the aforementioned triangular waveform of predetermined frequency. The clock 15 is used to measure time increments such that the variable pulse width may be counted.

The Vsync detector & phase shift detector 13 receives as inputs, Vsync 38, Sel1, Sel0, and a clock 15. Vsync 38 is an independent reference signal as discussed above. The Vsync detector & phase shift detector 13 detects the presence of an

independent reference signal, Vsync 38, and calculates a phase delay value, D, as described above. In the exemplary IC, if Vsync 38 is not detected, detector 13 utilizes the frequency of the oscillator 22 to generate a reference signal 38. When detector 13 detects a Vsync signal 38, the detector 13 abandons the oscillator 22 frequency and adopts the Vsync frequency for signal 38. Detector 13 outputs the phase delay value, D, as well the independent reference signal, 38. Signal 38 along with a clock 15 is fed into a frequency doubler 14, wherein the frequency of Vsync is doubled to generate the burst frequency.

In the exemplary IC, the inputs of phase delay array 16 include PWM signal 36 from PWM generator 12, a burst frequency value from frequency doubler 14 and a clock 15. As described above, the phase delay array 16 utilizes a counter to generate multiple phase delayed burst signals, wherein each phased burst signal operates to regulate power to a load 18. Each phased burst signal is driven through a buffer 19 to amplify its current driving capacity, and then through a respective phase array driver 100. This is discussed further below.

The protection circuitry 2 is used to sense the voltage level of a power source (Vcc). When Vcc, shown at pin 26 in Figure 6, increases from low to high, the protection circuit 2 resets the entire IC such that the IC is functionally at an initial status. When Vcc goes low, the protection circuit 2 shuts down the IC to prevent possible damage to the IC.

Figure 8 shows a top-level diagram of exemplary phase array drivers 100. In an exemplary configuration, each phase array driver, Driver 1, Driver 2, ... Driver n/2, receives two phased burst signals as inputs, and outputs power to two respective loads. The regulation of power to each load is independent of the regulation of power to the other loads. Therefore, alternative configurations allow for each phase array driver 100 to regulate any number of loads totaling more or less than as depicted in the figures. In an exemplary system, each phase array driver 100 receives two phased burst signals 50 which are 180° out of phase and generates two power regulating signals 51 which are 180° out of phase. Phase array drivers 100 translate each variable pulse width L into a duration for which a respective load stays on in each cycle. Therefore, the greater the pulse width of a phased burst signal, the greater the power delivered to the respective load during each cycle. Also each load turns on and

off at the burst frequency defined by the respective phased burst signal 50. Since driver 100 receives complementary signals in the exemplary system, the number of phased burst signals 50 is even for this embodiment.

Figure 9 provides an exemplary circuit 200 demonstrating the generation of a load current controlling signal, ICMP, in a phase array driver 100. Figure 10 is an accompanying timing diagram to Figure 9. Figures 9 & 10 are considered together in the following discussion. Also, references are made to Figures 1-5.

Circuit 200 comprises an error amplifier 120 generating the current controlling signal, ICMP, a sense resistor Rsense 138 coupled in series to a load 18, a switch 134 for coupling circuit 200 to the phase delay array 16, and a feedback capacitor CFB 139. Additionally, an exemplary circuit 200 includes an RC low-pass filter 136 for filtering noise, and utilizes a transformer 160 to apply the current controlling signal, ICMP, to the load 18. The above components are discussed further below.

Generally circuit 200 receives a feedback signal, VIFB, and generates the current controlling signal, ICMP, during two modes of operation. The first mode is soft start and the second mode is burst mode. In soft start mode, the load 18 is powered up from an off state to an operationally on state during a warm up period, utilizing an external soft start controller (not shown). The soft start controller is discussed further below. In burst mode, the duty cycle of the aforementioned phased burst signal 50 (PWM) is utilized to regulate load current, IL, during the operationally on state of the load 18. That is, in an exemplary embodiment, IL will be proportional to [L/(T/K)]*ILmax, where L is the pulse width of signal 50, T/k is the period of signal 50, and ILmax is the load current when the load is fully powered on. In this manner, a load 18 is dimmed during burst mode. This is discussed further below. Note that soft start mode sequentially precedes burst mode. The current controlling signal, ICMP, regulates load current, IL, during burst mode, but not during soft start. During soft start, ICMP is monitored to determine when to toggle modes from soft start to burst mode. This is explained further below.

In both modes, the error amplifier 120 compares the feedback signal, VIFB, with a reference signal, ADJ, and generates the controlling signal, ICMP. In an exemplary embodiment, error amplifier 120 is a negative feedback operational amplifier. ADJ is a predetermined constant reference voltage representing the

operational current of the load 18. This is discussed further below. ICMP varies to increase or decrease VIFB to equal ADJ. That is, if VIFB is less than ADJ, then the error amplifier 120 increases ICMP. Conversely, if VIFB is greater than ADJ, then the error amplifier 120 decreases ICMP. If VIFB=ADJ, ICMP is a constant to maintain VIFB at ADJ. The operations of exemplary circuit 200 during soft start mode and during burst mode are discussed in that order and in greater detail below.

As stated above, in soft start mode, the load 18 is powered up from an off state to an operationally on state. Circuit 200 generates the controlling signal, ICMP, based on the load current, IL, but not based on the respective phased burst signal, PWM 50. That is, during soft start, circuit 200 is decoupled from phase delay array 16 by switch 134. This is discussed further below. The following discussion proceeds with reference to ILrms and ILrms (spec). ILrms refers to the root mean square of the load current, IL at any given moment. ILrms (spec), as used herein, is the manufacturer's load specifications when the load 18 is operating at full power.

In soft start mode, the feedback signal, VIFB is a function of load current, IL. IL is generally a sinusoidal waveform. Following Ohm's Law, VIFB is proportional to Rsense * IL. VIFB approximately equals 0.45*Rsense*ILrms and is derived as follows.

$$ILrms = \sqrt{[\int_{t_1}^{t_1+T_L} (ILpeak * Sin(t))^2 dt] / T_L} = ILpeak / \sqrt{2}$$

where T_L is the period of the sinusoid, t_1 and $t+T_L$ respectively define the start and end points of one period of the sinusoid, and ILpeak is the peak load current. Diodes 137 filter out the negative portions of IL, thereby generating a waveform, IL(+), an example of which is illustrated by signal 400 in Figure 9a, which depicts the half-rectified current waveform delivered to the load. With the phased burst signal, PWM 50, decoupled from circuit 200, VIFB is effectively the voltage across Rsense. That is,

$$VIFB = [\int_{t_1}^{t_1+T_L} Rsense * IL(+) dt] / T_L$$

$$= (ILpeak * Rsense) / \pi$$

Since ILrms = ILpeak/$\sqrt{2}$,

$$VIFB = (\sqrt{2} / \pi) * ILrms * Rsense \approx 0.45 * ILrms * Rsense$$

The present invention is not to be limited by this method of determining feedback, VIFB. In the exemplary embodiment, in both soft start and burst modes, the constant reference voltage, ADJ, equals 0.45*ILrms(spec)*Rsense, where ILrms(spec) is generally a constant defined by the load's operational specifications as described above. Therefore, when the load 18 is at full power, i.e., on, as per operational specifications, VIFB will equal ADJ. Since the load 18 is turned on from an off state, at the initiation of soft start mode, IL is effectively zero. Consequently, VIFB is effectively zero, i.e. less than ADJ. Therefore, ICMP is high. As IL is increased by the soft start controller (not shown), VIFB increases, thereby reducing the difference between VIFB and ADJ. Consequently, ICMP decreases. When VIFB=ADJ, the load 18 is operationally on as described above, and ICMP carries the energy to regulate the load 18 at its operational current. Therefore, the warm up stage defined by the soft start mode concludes when the energy provided by the soft start controller (not shown) has increased to match that provided by ICMP. At this time, the soft start controller (not shown) ceases control, and ICMP regulates load current. Burst mode begins.

In burst mode, circuit 200 generates the controlling signal, ICMP, based on both the load current, IL, and PWM signal 50. Therefore, VIFB no longer adheres solely to the equation, VIFB=(0.45)*Rsense*ILrms. Instead, the above equation is supplemented by a factor determined by the presence of PWM signal 50. Consequently, in burst mode, ICMP follows the PWM signal 50 and drives the load 18. This is described further below.

Switch 134 couples circuit 200 to phase delay array 16 during burst mode. In an exemplary system, switch 134 is a PNP transistor 134 with a reference power source, REF, at its source (or emitter) and the respective phased burst mode signal (PWM) 50 at its gate (or base). The reference power of REF may be derived via a voltage divider circuit (not shown) dividing, for example, an exemplary IC source voltage, VCC (not shown). When triggered by PWM 50, switch 134 couples its drain (or collector) to the REF at its source, transmitting a signal, PWM_52, to circuit 200. In the preferred embodiment, the switch 134 is triggered by a low signal at its gate, and therefore, PWM_52 is complimentary to PWM 50. When PWM 50 is high, transistor 134 is off, and PWM_52 is isolated from PNP 134; that is, no burst mode

information is transmitted to circuit 200, and VIFB follows the equation, 0.45*ILrms*Rsense, in an exemplary embodiment. When PWM 50 is low, transistor 134 is on, and PWM_52 is high. Rlimit 135 translates PWM_52 current into voltage. This voltage is added to VIFB. Rlimit is chosen such that the voltage added into VIFB effects ICMP to vary load current from an operationally on state to an off state. This is discussed further below.

The PWM signal 50 is introduced and PWM_52 generated as described above. When PWM 50 goes low, PWM_52 goes high, and therefore, VIFB exceeds ADJ. To decrease VIFB and match VIFB to ADJ, ICMP goes low. Since ICMP drives the load 18, the load 18 effectively turns off. One skilled in the art will recognize that the load 18 being off does not require current or voltage to the load 18 to be zero; current or voltage may continue to charge the load 18 minimally when it is off. Then, when PWM 50 goes high, PWM_52 is decoupled from the reference voltage, REF. VIFB returns to the equation VIFB=0.45*ILrms*Rsense in the exemplary embodiment. Since the load is effectively off, ILrms approximates zero. ICMP goes high to build VIFB to approximate ADJ. Consequently, load current, IL, goes high, and the load 18 turns on. The result, as seen from Figure 10, is that load current, IL, follows the respective phased burst signal, PWM 50. However, that load current IL also lags the respective burst signal, PWM 50.

Figure 11 displays oscilloscope signal readouts of PWM_ 52, ICMP and load current IL during burst mode operation of an exemplary system of the present invention. PWM_52 is timed with the respective phased burst signal, PWM 50; that is, no significant delay exists between high-to-low or low-to-high transitions of PWM 50 and the respective low-to-high or high-to-low transitions of PWM_52. Because the error amplifier 120 has finite charge and discharge current, it takes time to charge or discharge CFB 139 when VIFB goes higher or lower than ADJ, respectively. Consequently, as seen in Figure 11, ICMP lags PWM_52. Since ICMP drives the load 18 during burst mode operation, load current, IL, likewise lags PWM_52.

Figure 12 provides an exemplary IC implementation 300 of a phase array driver 100. IC 300 comprises a break-before-make circuit 130 with a half-bridge switching topology. This is discussed further below. In alternative IC implementations, switching topologies such as "full bridge," "forward," or "push-

pull," can be used without departing from the scope of the present invention. Continuing references to Figure 9 are included to explain some operational aspects of IC 300. Exemplary IC 300 receives two phased burst signals (PWM signals) 50 which are 180 degrees out of phase with each other. Exemplary IC 300 utilizes these phased burst signals 50 to drive two respective loads whose signals are 180 degrees out of phase with each other. Thus, those skilled in the art will recognize duplication of certain components (e.g., selectors 122, 124 and 126) to drive two individual loads. Of course, IC 300 is only an example, and may be readily configured to drive three or more loads (or a single load). At the outset, description will be made to selectors 122, 124 and 126 which may be constructed from generic comparator circuitry and/or custom circuitry to accomplish the signal detection, as set forth below.

Exemplary IC 300 comprises an error amplifier 121 for voltage sensing, an error amplifier 120 for current sensing, a current or voltage feedback selector 122, a burst mode or soft start selector 124, and a minimum voltage selector 126. Selectors 122, 124, and 126 may be of the same structure, comprising 1 comparator and 2 transmission gates, and may be implemented with multiplexers.

As described above, each error amplifier 120 generates a current controlling signal, ICMP (shown at pin 4 in the exemplary IC 300) by comparing ADJ with feedback, VIFB (shown at pin 3 in the exemplary IC 300), determined by load current, IL, in soft start mode, and by both IL and phased burst signal, PWM 50, in burst mode.

Likewise, Figure 13 provides an exemplary circuit 350 showing an error amplifier 121 for generating a voltage controlling signal, VCMP (at pin 5 in the exemplary IC), by comparing a reference voltage (e.g., 2V) with a voltage feedback signal, VFB (at pin 6 in the exemplary IC 300) determined by load voltage. In an exemplary embodiment, when the load is initially powered on, power delivered to the load by the soft start controller (at input 132), heretofore referred to as SST, is low. That is, the load voltage, Vx, on the secondary side of transformer 160 is low. Consequently, VFB is low. Since the difference between VFB and the reference signal (e.g., 2V) is greater than the threshold of comparison, error amplifier 121 generates a high VCMP signal. The relationship between VFB and load voltage is discussed further below. As SST increases, VFB increases and approaches the

reference voltage (e.g., 2V), and VCMP decreases. When VFB matches the reference voltage (e.g., 2V), VCMP is chosen instead of SST to drive load voltage, effectively clamping the load voltage at a predetermined value such that VFB matches the reference voltage (e.g., 2V). Circuitry 360 illustrates the relationship between VFB, and the actual load voltage, Vx, provided at the secondary side of the transformer, in the exemplary circuit 350:

$$VFB = Vx * C1/(C1+C2)$$

Therefore, C1 and C2 are chosen such that VFB, the voltage feedback signal, reflects a desired factor of load voltage, Vx. For example, if C2 = 1000 * C1, then, VFB = Vx/1000, that is, VFB is a representation of load voltage which is $1/1000^{th}$ of load voltage, Vx. In this example, if the reference voltage is 2 Volts, then, the load voltage is clamped at 2000 Volts. Further, analogous to half-wave rectifier diodes 137 of Figure 9, diodes 365 generate a half wave rectified voltage signal. Ry and Cy are peak voltage detectors to detect the peak voltage of the rectified waveform.

The current or voltage feedback selector 122 (I_or_V Feedback), selects either the voltage controlling signal, VCMP, or current controlling signal, ICMP, as the signal to drive the load during burst mode operation. In an exemplary IC 300, selector 122 chooses VCMP if load voltage exceeds the aforementioned predetermined value while load current is less than the operational current (i.e., VIFB < ADJ). Otherwise, selector 122 selects ICMP. Selector 122 may utilize alternative comparisons to determine the selection of a controlling signal, for example, selector 122 could be configured to compare ADJ and VIFB to determine if the load has reached operational or predetermined full power. The following discussion proceeds with reference to a controlling signal, CMP, which may either be ICMP or VCMP as described above.

In the exemplary IC 300, selector 122 is coupled to the burst mode or soft start selector 124 (CMP_OR_SST). Selector 124 of the exemplary IC 300 determines which of the aforementioned two modes of operation apply, i.e., soft start or burst mode, and toggles from soft start to burst mode when appropriate, as follows. Selector 124 compares CMP and SST (the load power controlling energy generated by the soft start controller) to determine which mode applies and to generate a signal, CMPR, which is either the soft start signal, SST, in soft start mode, or the controlling

signal, CMP, in burst mode. Since, as described above, burst mode is triggered once the load 18 has reached an operationally on state, CMPR is SST prior to SST equaling CMP, and CMPR is CMP once SST equals or exceeds CMP. The soft start controller which provides for the soft start signal (SST) is implemented, for example, by using a capacitor (not shown) externally coupled to pin 13, 132, whose charging rate determines the rate at which the load is powered up. In this example, SST voltage equals Is/(C*T) where I_s is the current supplied by power source 133 and C is the capacitance of the external capacitor (not shown). The capacitance of the external capacitor (not shown) may be varied to vary the rate at which load current, IL, is increased during soft start mode. Although soft start mode ends and burst mode begins when CMP matches SST, and CMP regulates power to the load during burst mode, SST continues to increase to VCC.

Selector 124 is coupled to a minimum voltage selector, CMPR_or_MIN 126, in the exemplary IC 300. The output of selector is herein referred to as RESCOMP. Selector 126 ensures that a predetermined minimum power is delivered to the load, even when the load is in an "off" state. That is, when power delivered to the load is less than a predetermined minimum value, RESCOMP is a minimum voltage, for example, 740mV. If the load voltage is above the predetermined minimum voltage, then RESCOMP is CMPR (i.e., either CMP or SST as described above).

Consequently, in burst mode, whenever PWM 50 goes low and the load turns off as described above, a predetermined minimum voltage is maintained across the load. The desirability of maintaining a minimum voltage across the load is explained below with reference to a CCFL (Cold Cathode Fluorescent Lamp) as an exemplary load.

A CCFL is of high impedance when off. Thus, a large voltage is needed to initially induce current through the lamp, that is, to turn on the lamp. In the exemplary IC 300, a large voltage is applied to the CCFL, by the secondary side of transformer 160, to turn on the lamp. Once current has been induced through the lamp, the impedance is decreased, and consequently, voltage may be decreased to operational levels. The predetermined minimum power is maintained across the load thereafter to avoid having to repeat the application of a large voltage to turn on the lamp.

When a predetermined minimum voltage is selected by selector 126, ramp 128 functions as a pulse width modulator (PWM) and generates a PWM signal with pulse width determinative of power to the load. The functionality of ramp 128 is analogous to that of pulse width modulator 12 discussed in relation to Figure 3. With reference to this analogy, the DC voltage utilized by the ramp 128 for the generation of the PWM signal is the predetermined minimum voltage. The predetermined minimum voltage, in intersection with the triangular signal 34 discussed in relation with Figure 3, generates a PWM pulse width that is minimally adequate to maintain a signal. Effectively, ramp 128 utilizes the predetermined minimum voltage supplied by selector 126, to leave the load minimally powered on when the load is off, during each burst cycle. Where the load voltage is in excess of the predetermined minimum, the power signal determined by aforementioned burst signal PWM 50 is utilized.

Break-before-make circuit 130 utilizes the appropriate signals described above to turn a transformer 160 on and off. Note that, alternatively, any suitable switch may be used for this purpose. The exemplary IC 300 includes two switches used in a half-bridge topology, i.e., as a general-purpose DC/AC converter, the outputs of the break-before-make circuit 130, NDRI and PDRI, turn on or off an NMOSFET and PMOSFET respectively, thereby switching a transformer 160 to ground or to VCC (power supply) respectively. Significantly, the break-before-make circuit ensures that the NMOSFET and PMOSFET each turn on exclusively as to the other. That is, the NMOSFET and PMOSFET generate a pair of non-overlapped signals. In an alternative embodiment, four switches are used in a full bridge (H-bridge) topology to switch the transformer 160 to ground or to VCC. The switches convert the DC rail voltage (VCC) to an AC signal which is supplied to the primary side of the transformer, as is well known to those skilled in the art.

Figures 14(a) and 14(b) are circuit examples of conventional DC/AC converter topologies using half bridge and full bridge switching schemes, respectively. The half bridge topology exemplified by Figure 14(a) is provided in the exemplary IC 300 and described above. An alternative embodiment utilizes a full bridge (H-bridge) topology exemplified by Figure 14(b). The full bridge topology typically utilizes two NMOSFET and PMOSFET pairs generating two pairs of non-overlapped signals. This is described below with reference to Figure 15. The transformer 160 is turned on

or off by alternating the conduction of pairs of crossed switches, A and D (AD), and B and D (BD), respectively. The break-before-make circuit 130 ensures that AD and BC are not on at the same.

Figure 15 provides a signal generation example showing the generation of crossed switch signals (i.e., AD and BC signals) in a full-bridge topology of an exemplary embodiment of the present invention. As discussed in reference to Figure 3, oscillator 22 generates the triangular signal 34. Signal 34 is inverted to generate signal 34'. RESCOMP is the output of selector 126. That is, RESCOMP is one of ICMP, VCMP, SST, or MIN (e.g., 740mV). Therefore, RESCOMP is variable. A reference signal, CLK, is utilized to independently toggle switches A and B. In an exemplary embodiment, CLK has a 50% duty cycle and follows signal 34. A second reference signal, PS_CLK, is utilized to independently toggle switches C and D. In the exemplary embodiment, PS_CLK is a CLK signal phased by an adjustable delay, D_{clk}. RESCOMP determines D_{clk}. This is discussed as follows. The positive and negative edge of each pulse of PS_CLK are generated by the respective intersection of the rise of signal 34 and RESCOMP and the respective intersection of rise of signal 34' and RESCOMP. Therefore, when RESCOMP increases, as, for example, when the respective phased burst signal 50 goes high during burst mode, the phase delay, D_{clk}, between CLK and PS_CLK increases. The on times of switching pairs, AD and BC, are determined by the overlaps of CLK and PS_CLK. Therefore, when D_{clk} increases, the on times of AD and BC increase, thereby causing more power to be delivered to the respective load. Note, however, that the present invention is not limited by any particular driver architecture, and therefore, not limited to half-bridge or full-bridge topologies.

Returning to IC 300 of Figure 12, in the exemplary embodiment, where voltage supplied to the transformer 160 exceeds the source voltage to the IC 300, the break-before-make circuit 130 utilizes "High Voltage Level Shifting". "High voltage level shifting" is explained by the following example. VCC is 5 volts. That is, PMOSFET gate control signal levels vary from ground (0 volts) to VCC (5 volts). If 15 volts are fed into the transformer 160, the break-before-make circuit 130 provides a DC voltage shift of 10 volts to the PDRI output, thereby allowing for the PMOSFET

gate control signal to reach 15 volts (10 volts via DC high voltage level shifting + 5 volts VCC).

Exemplary IC 300 further includes protection circuitry 140. In this IC 300, circuitry 140 is an under voltage lock out circuit (UVLO). At the end of soft start mode, if the voltage delivered to the transformer 160 does not decrease, or if load current, IL, does not reach the specified full operational level, circuitry 140 shuts down IC 300. Primarily, circuitry 140 senses load current and shuts down IC 300 during burst mode operation if VIFB is lower than ADJ while maximum power is being delivered to the load. Note that when VIFB is lower than ADJ, error amplifier 120 increases output power to the load as discussed above. Therefore, circuitry 140 shuts down the IC upon the above condition in order to prevent damage to components from excessive power delivery. Also, protection circuitry 140 is disabled during the soft start duration described above.

Thus, it is evident that there has been provided a sequential burst mode regulating circuit that satisfies the aims and objectives stated herein. Those skilled in the art will recognize numerous modifications that can be made to the present invention, and all such modifications are deemed within the spirit and scope of the present invention, only as may be limited by the appended claims.

CLAIMS

1. A variable power regulator, comprising:

a pulse modulator generating a pulse signal having a pulse width; and

a phase delay array receiving said pulse signal and a frequency selection signal, and generating a plurality of phased burst signals, each having a frequency determined by said frequency selection signal wherein at least two of said phased burst signals have different start times.

2. A circuit as claimed in claim 1, wherein each said phased burst signal of said plurality of phased burst signals regulates a respective load.

3. A circuit as claimed in claim 1, wherein said pulse modulator includes a variable selector for selecting said pulse width.

4. A circuit as claimed in claim 3, wherein said variable selector comprises a dimmer providing a DC signal, and an oscillator generating a triangular waveform, wherein said pulse width being determined by the intersection of said DC signal and said triangular waveform.

5. A circuit as claimed in claim 4, wherein said dimmer further comprising a dim selector for setting the DC value of said DC signal, and a polarity selector for determining the section, of said intersection of said DC signal and said triangular waveform, to be used for generating the pulse width of said pulse width modulated signal.

6. A circuit as claimed in claim 1, further comprising a frequency selector receiving a reference signal and generating said frequency selection signal based on said reference signal, wherein said phase delay array receiving said frequency selection signal and setting the frequency of said pulse signal to said frequency selection signal.

7. A circuit as claimed in claim 1, wherein said phase delay array includes a counter for timing each said phased burst signal of said plurality of phased burst signals such that at least two of said phased burst signals have different start times.

8. A circuit as claimed in claim 1, wherein each said phased burst signal has a pulse width equal to said pulse width of said pulse signal.

9. A circuit as claimed in claim 1, wherein said phase delay array includes a phase delay generator for generating at least one phase delay value.

10. A circuit as claimed in claim 9, wherein said at least one phase delay value is a constant.

11. A circuit as claimed in claim 1, wherein said phase delay array includes at least one select signal input for determining the number of said phased burst signals to generate.

12. A circuit as claimed in claim 1, further comprising at least one phase array driver receiving at least one said phased burst signal and generating at least one respective power regulating signal for at least one respective load, said power regulating signal having a phase value equal to the phase value of said phased burst signal.

13. A circuit as claimed in claim 12, wherein each phase array driver receives two said phased burst signals which are 180° out of phase and generates two respective power regulating signals which are 180° out of phase.

14. A circuit as claimed in claim 12, wherein said phase array driver further comprising soft start circuitry generating power to said at least one respective load during a soft start period, wherein a soft start period defining a period wherein said at least one load is powered from an OFF state to an operationally ON state; and wherein once said load is at least at an operationally ON state, power to said load is regulated by said respective phased burst signal during a burst mode period.

15. A circuit as claimed in claim 12, wherein said phase array driver further comprising at least one comparator for limiting voltage of said at least one load to a predetermined voltage.

16. A circuit as claimed in claim 14, wherein said phase array driver including at least one error amplifier, receiving a feedback from said load during said soft start period, and further, receiving feedback from said at least one phased burst signal, wherein said error amplifier generates said at least one respective power regulating signal.

17. A circuit as claimed in claim 12, wherein said phase array driver further comprising at least one current or voltage feedback selector for selecting either to regulate current to said at least one respective load or regulate the voltage of said at least one respective load.

18. A circuit as claimed in claim 17, wherein said at least one current or voltage feedback selector comprises a multiplexer.

19. A circuit as claimed in claim 14, wherein said phase array driver further comprising a selector for selecting either said soft start period or said burst mode period.

20. A circuit as claimed in claim 19, wherein said selector comprises a multiplexer.

21. A circuit as claimed in claim 12, wherein said phase array driver further comprising a minimum voltage selector to regulate power to said at least one respective load with a selected current or minimum voltage.

22. A circuit as claimed in claim 21, wherein said selector comprises a multiplexer.

23. A circuit as claimed in claim 12, wherein said phase array driver further comprising a ramp circuit to deliver power to said at least one load.

24. A circuit as claimed in claim 12, wherein said phase array driver further comprising a DC/AC converter circuitry for generating an AC signal for at least one respective load.

25. A circuit as claimed in claim 24, wherein said converter includes a transformer for delivering a high voltage to said load based on said AC signal.

26. A circuit as claimed in claim 12, wherein said phase array driver further comprising protection circuitry for under voltage lock out.

27. A method for generating phase shifted burst mode signals, comprising the steps of:

generating a pulse signal having a pulse width;

generating a frequency selection signal;

generating a plurality of phased burst signals having a frequency of said frequency selection signal and said pulse width of said pulse signal; and

delaying at least one of said phased pulse signals to have a different start time than at least one other of said phased burst signals.

28. A method as claimed in claim 27, further comprising the step of:

regulating power to a plurality of loads using said plurality of said phased burst signals, respectively.

29. A method as claimed in claim 27, further comprising the step of:

generating a constant phase delay between each said phased burst mode signal.

30. A method as claimed in claim 28, wherein said step of generating a constant phase delay between each said phased burst mode signal comprising the step of dividing the period of said frequency selection signal by the number of loads utilized in said plurality of loads to generate a value for said constant phase delay.

31. A phased burst mode dimming system, comprising:

a pulse width modulator generating a pulse width modulated signal;

a variable selector for selecting the width of said pulse width modulated signal; and

a phase delay array receiving said pulse modulated signal and said frequency selection signal, and generating a plurality of phased burst signals by generating a phase delay between at least two said pulse width modulated signals.

32. A circuit as claimed in claim 31, wherein said variable selector comprises a dimmer providing a DC signal, and an oscillator generating a triangular waveform, wherein said pulse width being determined by the intersection of said DC signal and said triangular waveform.

33. A circuit as claimed in claim 32, wherein said dimmer further comprising a dim selector for setting the DC value of said DC signal, and a polarity selector for determining the section, of said intersection of said DC signal and said triangular waveform, to be used for generating the pulse width of said pulse width modulated signal.

34. A circuit as claimed in claim 31, further comprising a frequency selector receiving a reference signal and generating a frequency selection signal, wherein said phase delay array receiving said frequency selection signal and setting the frequency of said pulse signal to said frequency selection signal.

35. A circuit as claimed in claim 31, wherein said phase delay array includes a counter for timing each said phased burst signal of said plurality of phased burst signals such that at least two of said phased burst signals have different start times.

36. A circuit as claimed in claim 31, wherein each said phased burst signal has a pulse width equal to said pulse width of said pulse signal.

37. A circuit as claimed in claim 31, wherein said phase delay array includes a phase delay generator for generating at least one phase delay value.

38. A circuit as claimed in claim 37, wherein said at least one phase delay value is a constant.

39. A circuit as claimed in claim 31, wherein said phase delay array includes at least one select signal input for determining the number of said phased burst signals to generate.

40. A circuit as claimed in claim 31, further comprising at least one phase array driver receiving at least one said phased burst signal and generating at least one respective power regulating signal for at least one respective load, said power regulating signal having a phase value equal to the phase value of said phased burst signal.

41. A circuit as claimed in claim 40, wherein each phase array driver receives two said phased burst signals which are 180° out of phase and generates two respective power regulating signals which are 180° out of phase.

42. A circuit as claimed in claim 40, wherein said phase array driver further comprising soft start circuitry generating power to said at least one respective load during a soft start period, wherein a soft start period defining a period wherein said at least one load is powered from an OFF state to an operationally ON state; and wherein once said load is at least at an operationally ON state, power to said load is regulated by said respective phased burst signal.

43. A circuit as claimed in claim 40, wherein said phase array driver further comprising a comparator for limiting voltage of said at least one load to a predetermined voltage.

44. A circuit as claimed in claim 42, wherein said phase array driver further comprising at least one error amplifier, receiving a feedback from said load during said soft start period, and further, receiving feedback from said at least one phased burst signal, wherein said error amplifier generates said at least one respective power regulating signal.

45. A circuit as claimed in claim 40, wherein said phase array driver further comprising at least one current or voltage feedback selector for selecting either to

regulate current to said at least one respective load or regulate the voltage of said at least one respective load.

46. A circuit as claimed in claim 42, wherein said at least one current or voltage feedback selector comprises a multiplexer.

47. A circuit as claimed in claim 42, wherein said phase array driver further comprising a selector for selecting either said soft start period or said burst mode period.

48. A circuit as claimed in claim 42, wherein said at least one burst mode selector comprises a multiplexer.

49. A circuit as claimed in claim 40, wherein said phase array driver further comprising a minimum voltage selector to regulate power to said at least one respective load with a selected current or minimum voltage.

50. A circuit as claimed in claim 49, wherein said selector comprises a multiplexer.

51. A circuit as claimed in claim 40, wherein said phase array driver further comprising a ramp circuit to deliver power to said at least one load.

52. A circuit as claimed in claim 40, wherein said phase array driver further comprising a DC/AC converter circuit generating an AC signal to supply power to at least one respective load.

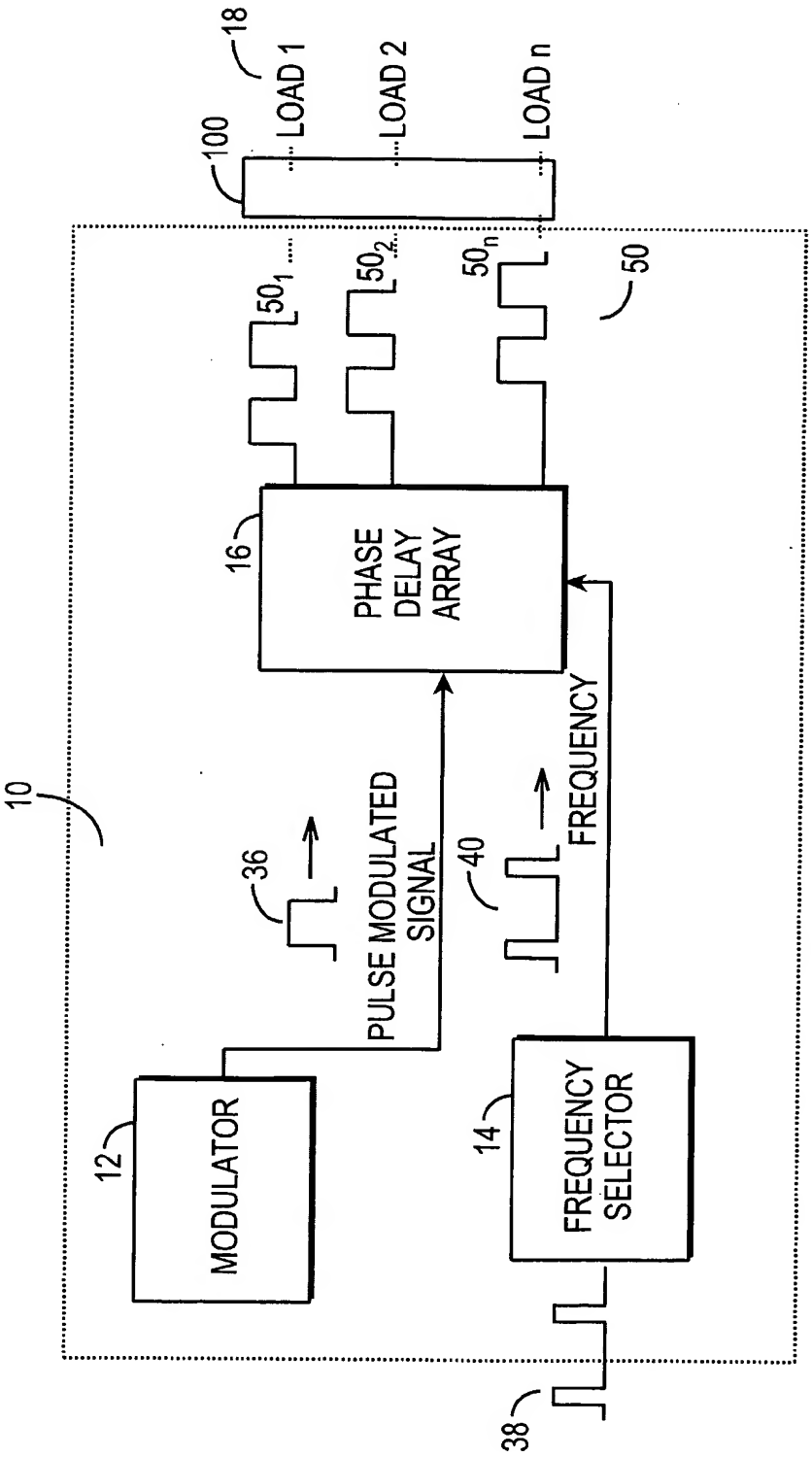
53. A circuit as claimed in claim 52, wherein said converter includes a transformer for delivering high voltage to said load based on said AC signal.

54. A circuit as claimed in claim 40, wherein said phase array driver further comprising protection circuitry for under voltage lock out.

55. A circuit as claimed in claim 6, wherein said frequency selector comprises a frequency doubler, doubling the frequency of said reference signal, and generating said frequency selection signal having a period twice that of said reference signal.

56. A circuit as claimed in claim 34, wherein said frequency selector comprises a frequency doubler, doubling the frequency of said reference signal, and generating said frequency selection signal having a period twice that of said reference signal.

FIG. 1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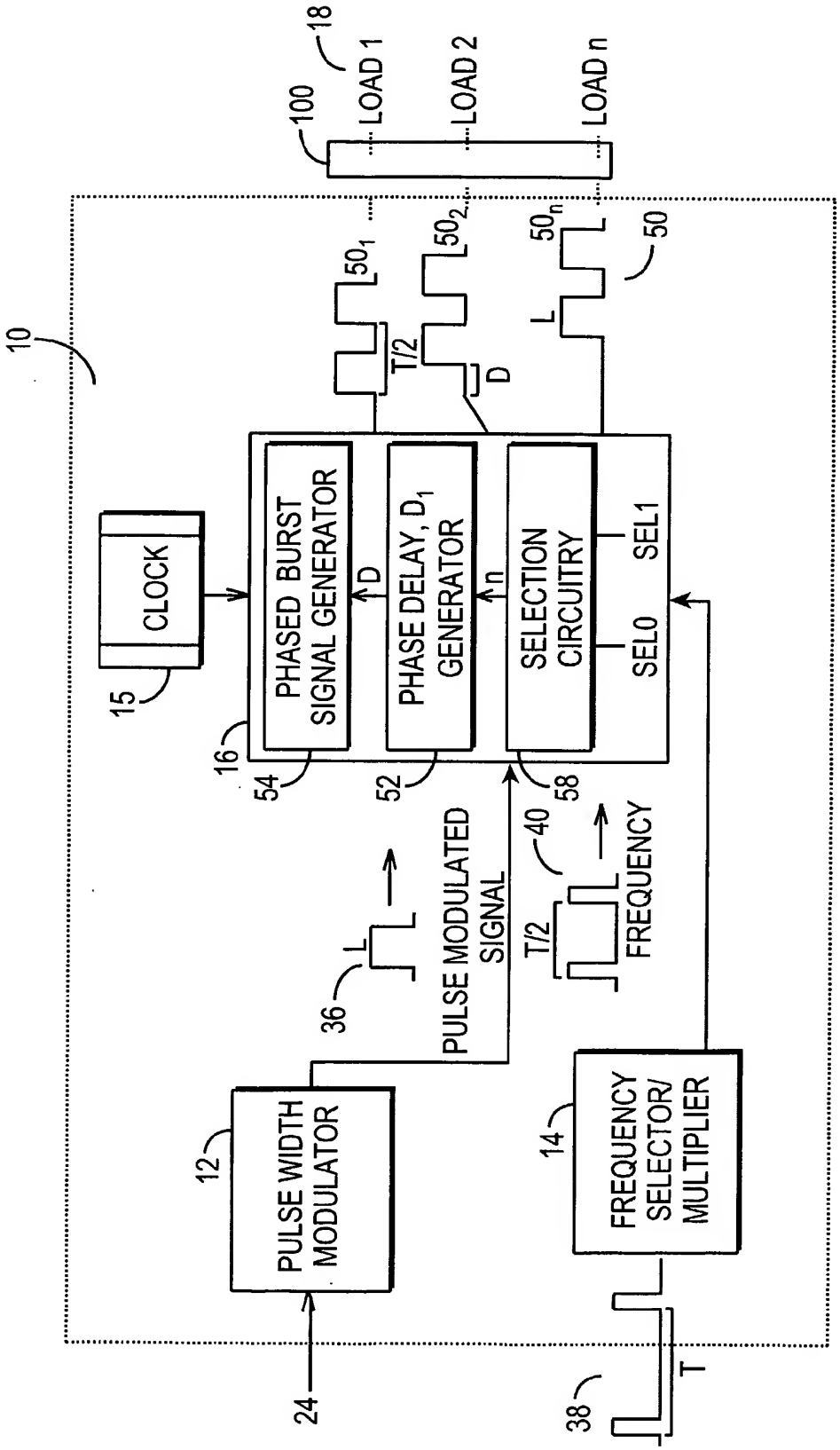
LOAD 2
LOAD n
100
50_1
50_2
50_n
50
16
PHASE DELAY ARRAY
10
36
PULSE MODULATED SIGNAL
40
FREQUENCY
12
MODULATOR
14
FREQUENCY SELECTOR
38

FIG. 2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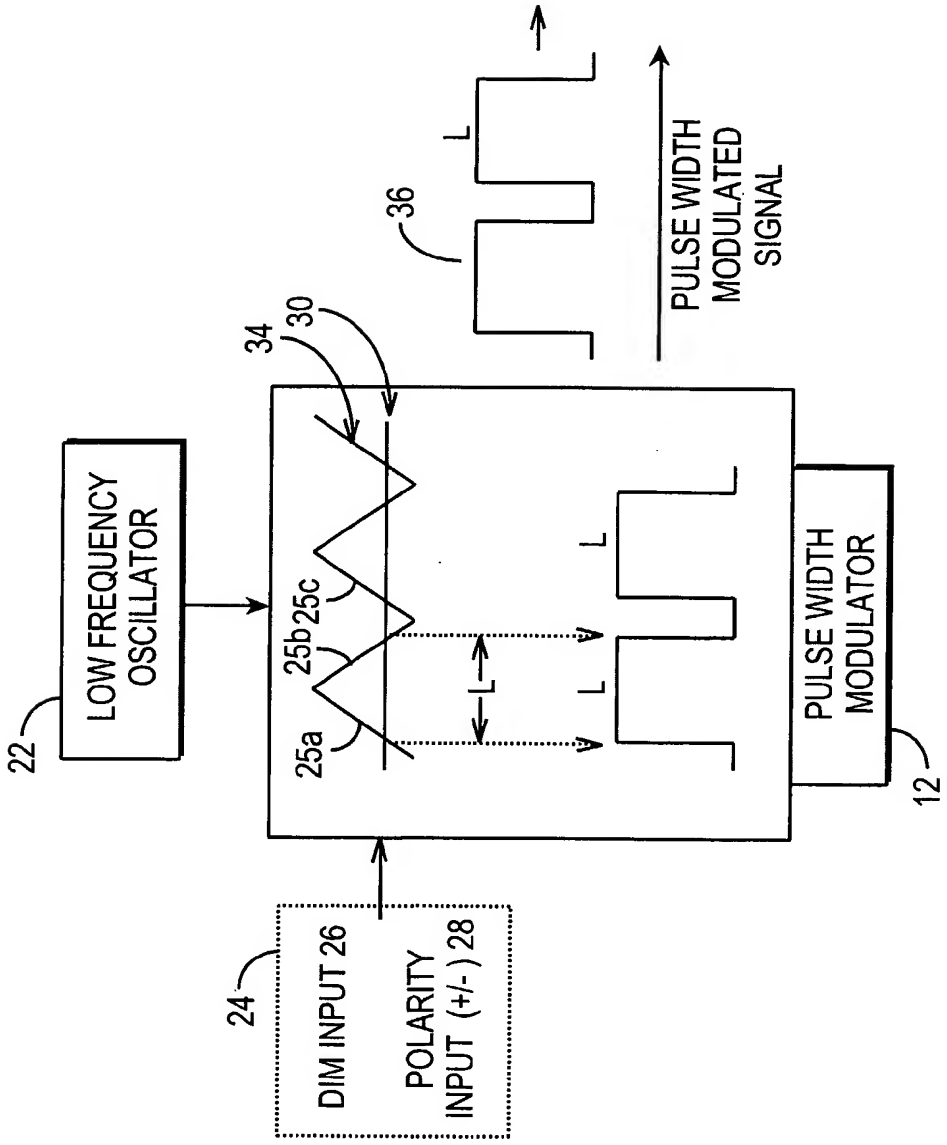
LOAD 1
LOAD 2
LOAD n
50
50_1
50_2
50_n
T/2
D
L
CLOCK
15
PHASED BURST SIGNAL GENERATOR
PHASE DELAY, D_1 GENERATOR
SELECTION CIRCUITRY
SEL1
SEL0
16
54
52
58
D
n
36
L
PULSE MODULATED SIGNAL
40
T/2
FREQUENCY
12
PULSE WIDTH MODULATOR
14
FREQUENCY SELECTOR/ MULTIPLIER
24
38
T

FIG. 3


LOW FREQUENCY OSCILLATOR
22
25a
25b
25c
L
L
L
L
34
30
36
PULSE WIDTH MODULATED SIGNAL
PULSE WIDTH MODULATOR
12
24
DIM INPUT 26
POLARITY INPUT (+/-) 28

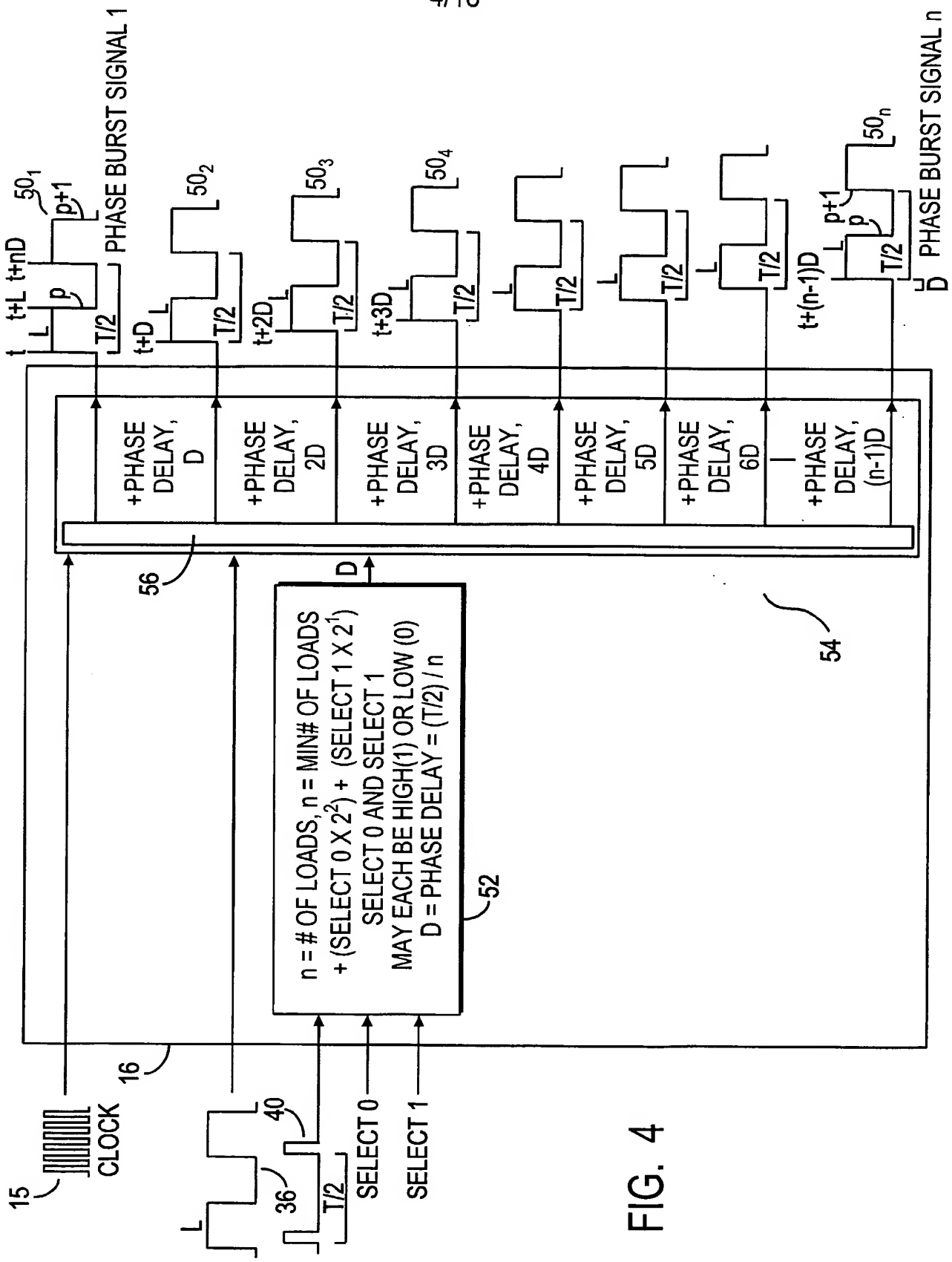

PHASE BURST SIGNAL 1
PHASE BURST SIGNAL n
+PHASE DELAY, D
+PHASE DELAY, 2D
+PHASE DELAY, 3D
+PHASE DELAY, 4D
+PHASE DELAY, 5D
+PHASE DELAY, 6D
+PHASE DELAY, (n-1)D
n = # OF LOADS, n = MIN# OF LOADS + (SELECT 0 X 2^2) + (SELECT 1 X 2^1)
SELECT 0 AND SELECT 1 MAY EACH BE HIGH(1) OR LOW (0)
D = PHASE DELAY = (T/2) / n
CLOCK
SELECT 0
SELECT 1
T/2
t
t+L
t+nD
t+D
t+2D
t+3D
t+(n-1)D
p
p+1
15
16
36
40
52
54
56

FIG. 4

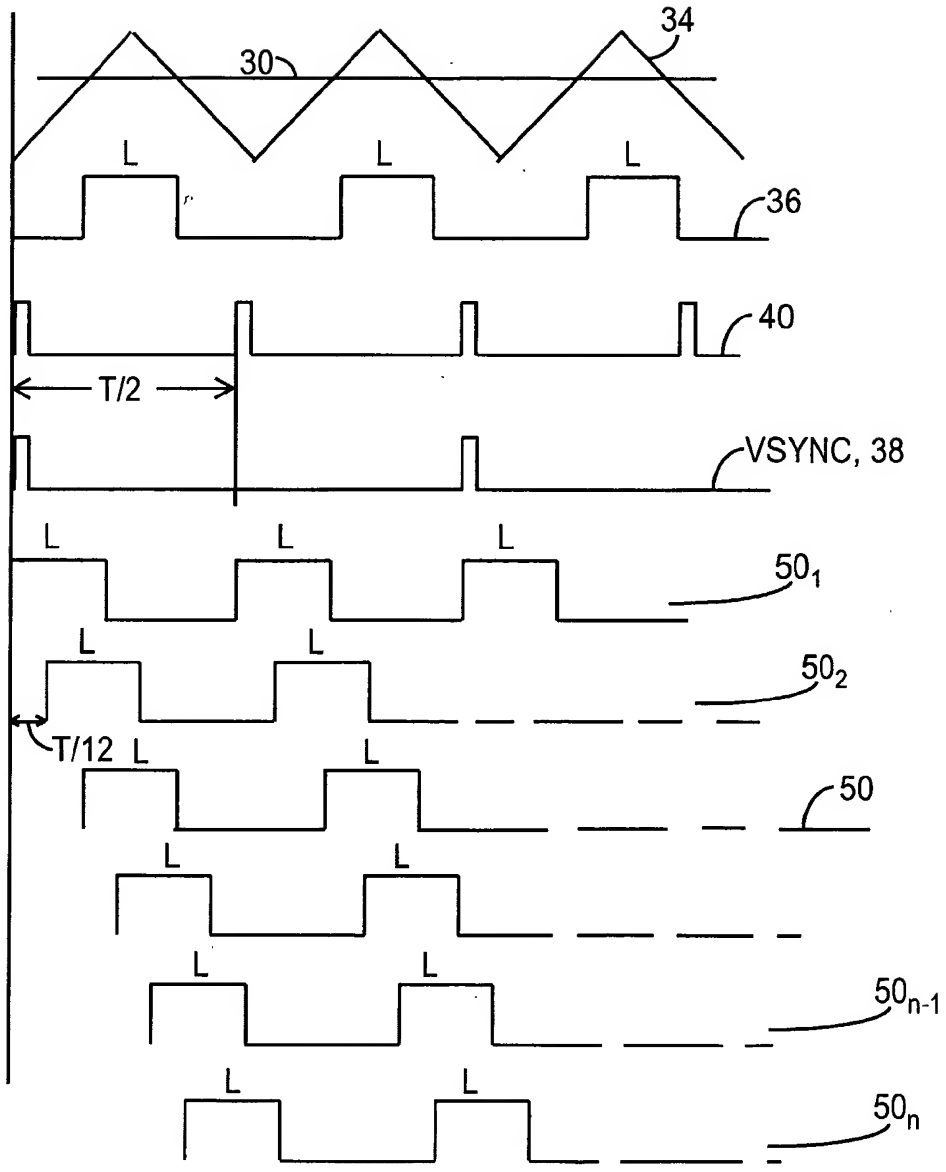
FIG. 5(a)

Sel0 (SELECT 0)	0	0	1	1
Sel1 (SELECT1)	0	1	0	1
n (# OF CCFLs)	6 (OR MIN #)	8 (MIN # +2)	10 (MIN # $+2^2$)	12 (MIN # $+2+2^2$)

FIG. 5(b)

Sel0	0	1	0	1	0	1	0	1
Sel1	0	0	1	1	0	0	1	1
Sel2	0	0	0	0	1	1	1	1
n (# OF LOADS)	MIN + 0	MIN + 2	MIN + 4	MIN + 6	MIN + 8	MIN + 10	MIN + 12	MIN + 14

FIG. 6


34
30
L
L
L
36
40
T/2
VSYNC, 38
L
L
L
50_1
L
L
50_2
T/12
L
L
50
L
L
L
L
50_{n-1}
L
L
50_n

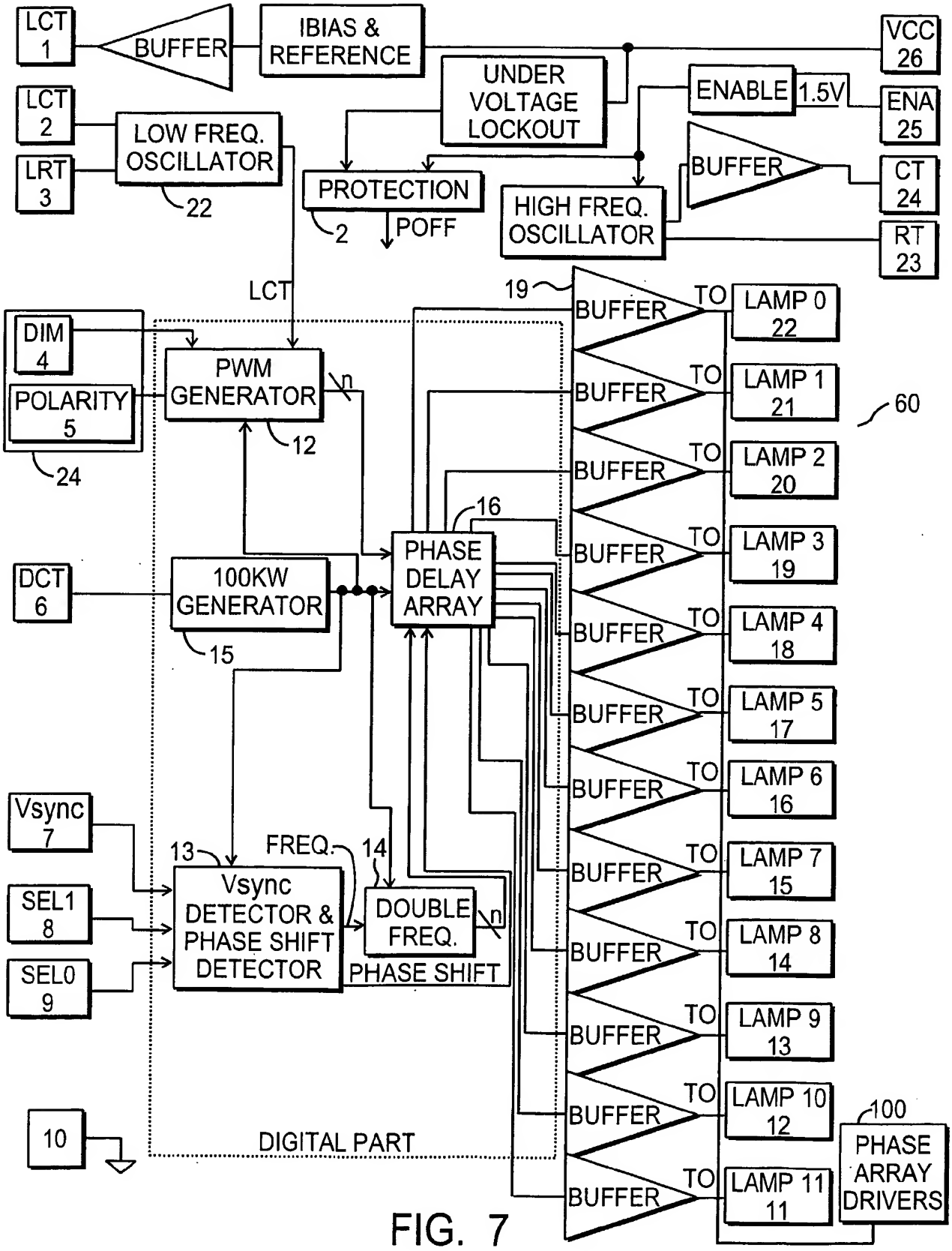

LCT 1
BUFFER
IBIAS & REFERENCE
VCC 26
LCT 2
LRT 3
LOW FREQ. OSCILLATOR
22
UNDER VOLTAGE LOCKOUT
ENABLE
1.5V
ENA 25
PROTECTION
2
POFF
HIGH FREQ. OSCILLATOR
BUFFER
CT 24
RT 23
LCT
19
DIM 4
POLARITY 5
24
PWM GENERATOR
n
12
BUFFER
TO
LAMP 0 22
LAMP 1 21
LAMP 2 20
LAMP 3 19
LAMP 4 18
LAMP 5 17
LAMP 6 16
LAMP 7 15
LAMP 8 14
LAMP 9 13
LAMP 10 12
LAMP 11 11
60
16
PHASE DELAY ARRAY
DCT 6
100KW GENERATOR
15
Vsync 7
SEL1 8
SEL0 9
13
FREQ.
14
Vsync DETECTOR & PHASE SHIFT DETECTOR
DOUBLE FREQ.
n
PHASE SHIFT
10
DIGITAL PART
100
PHASE ARRAY DRIVERS

FIG. 7

FIG. 8

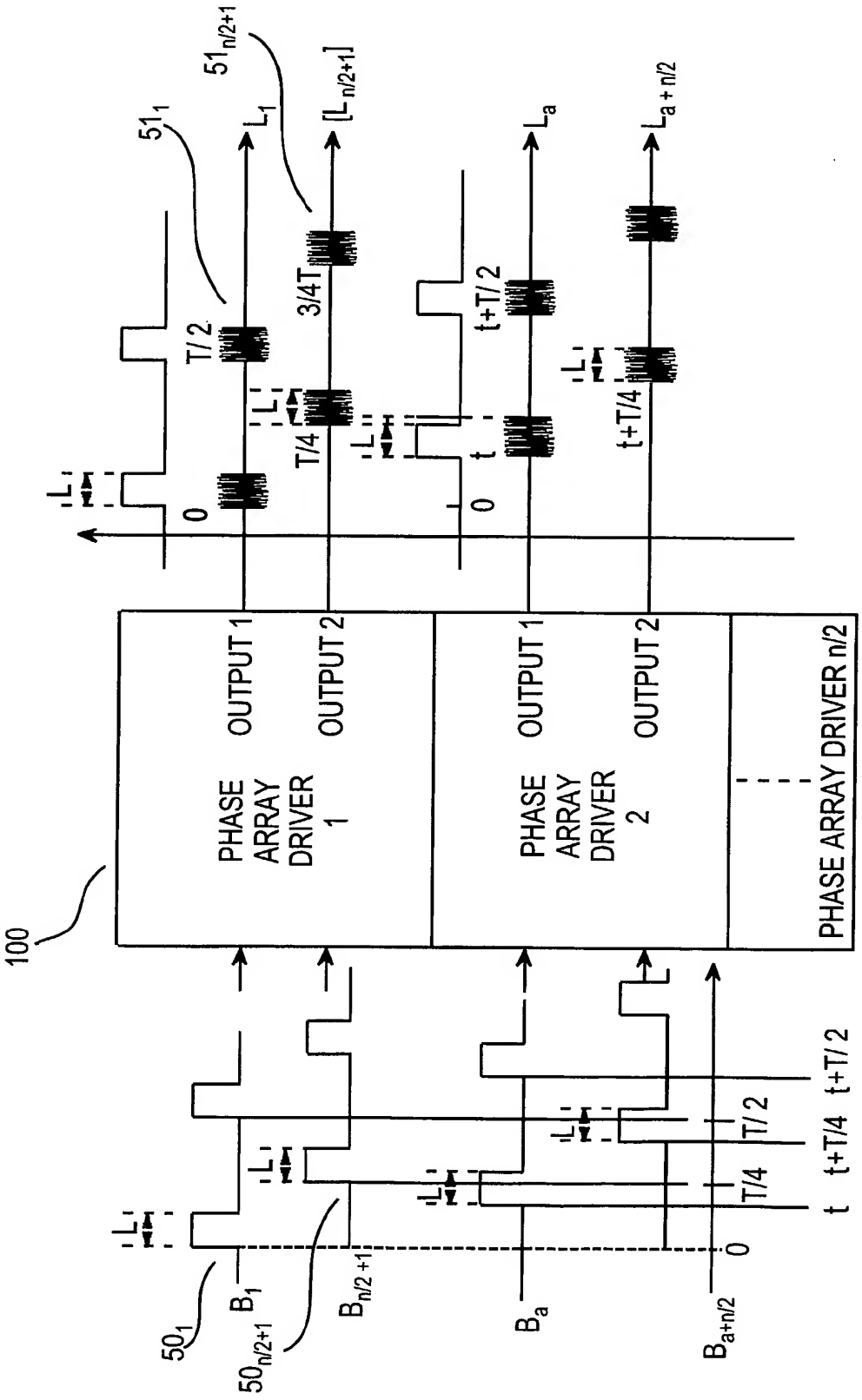

100
PHASE ARRAY DRIVER 1
OUTPUT 1
OUTPUT 2
PHASE ARRAY DRIVER 2
OUTPUT 1
OUTPUT 2
PHASE ARRAY DRIVER n/2
51 1
51 n/2+1
L 1
[L n/2+1]
L a
L a + n/2
T/2
T/4
3/4T
t+T/2
t+T/4
0
t
50 1
50 n/2+1
B 1
B n/2 +1
B a
B a+n/2
T/2
T/4
t t+T/4 t+T/2

FIG. 9

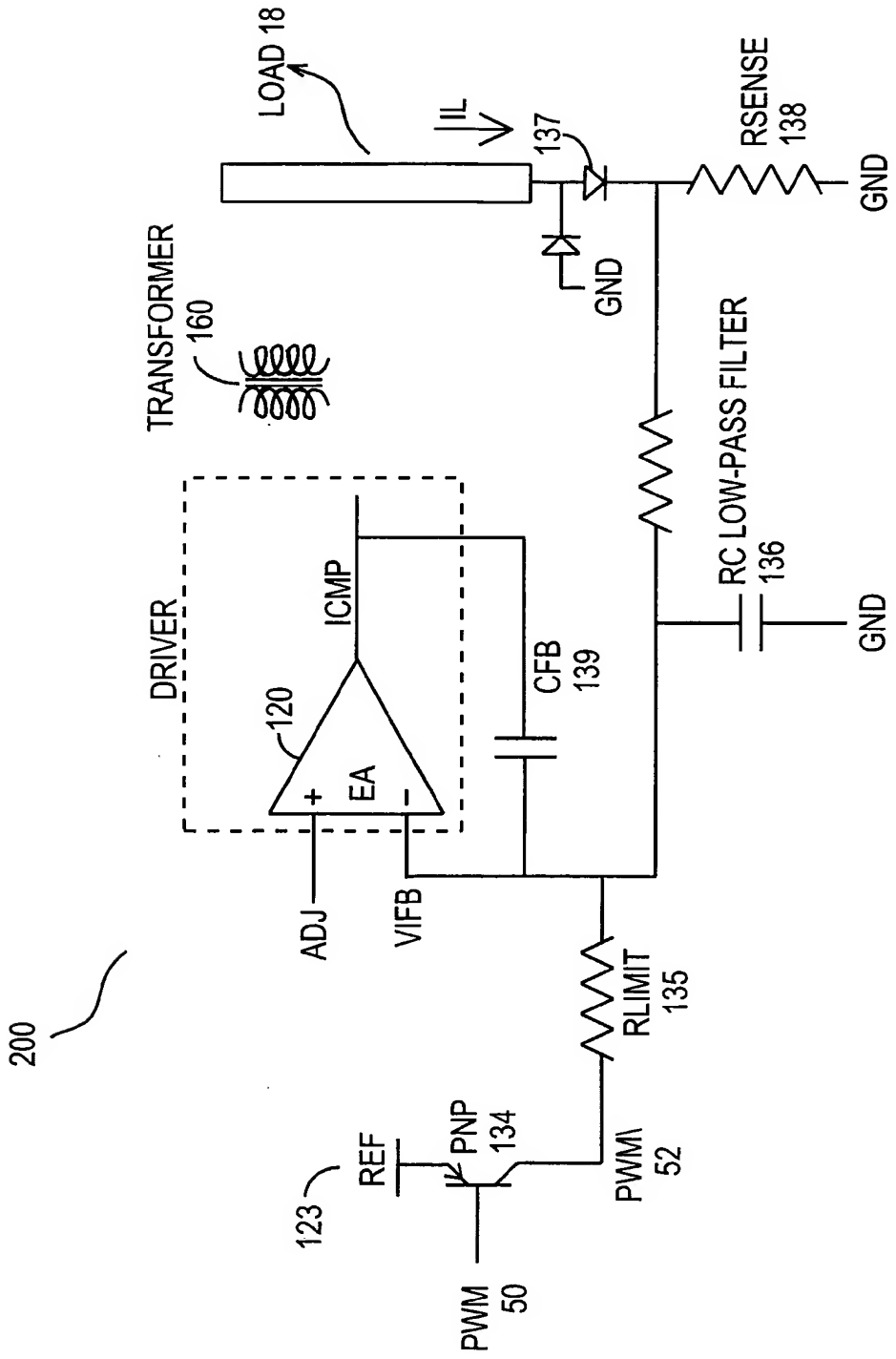

LOAD 18
IL
137
RSENSE
138
GND
GND
TRANSFORMER
160
RC LOW-PASS FILTER
136
GND
DRIVER
ICMP
CFB
139
120
EA
+
-
ADJ
VIFB
RLIMIT
135
200
REF
PNP
134
PWM\
52
123
PWM
50

FIG. 9a

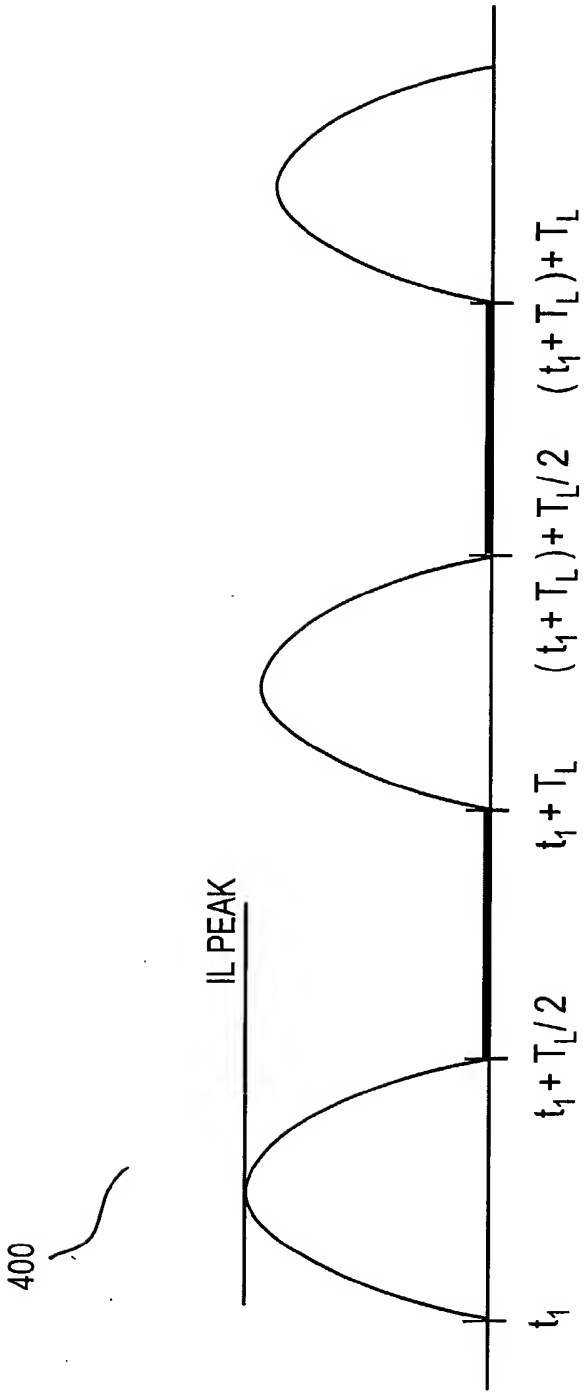


FIG. 10

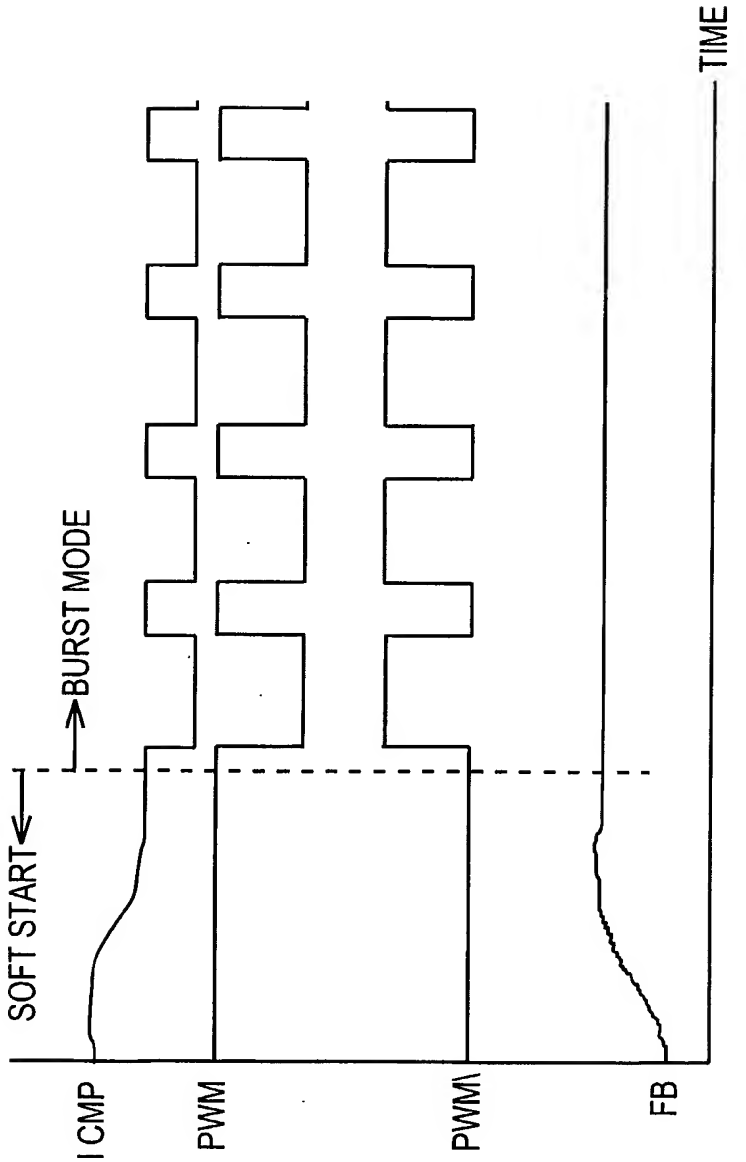
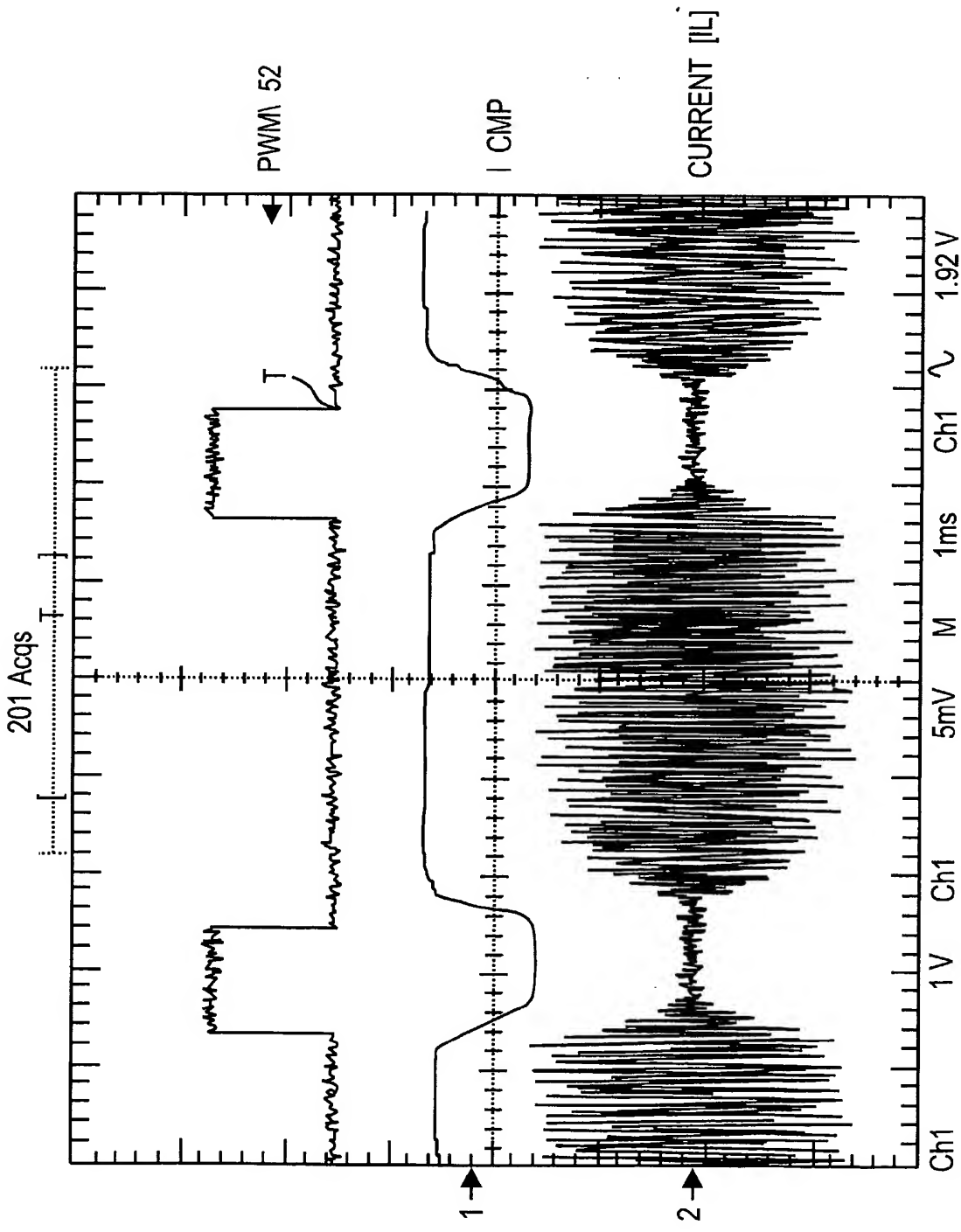


FIG. 11


PWM\ 52
I CMP
CURRENT [IL]
201 Acqs
T
T
1
2
Ch1
1 V
Ch1
5mV
M
1ms
Ch1
1.92 V

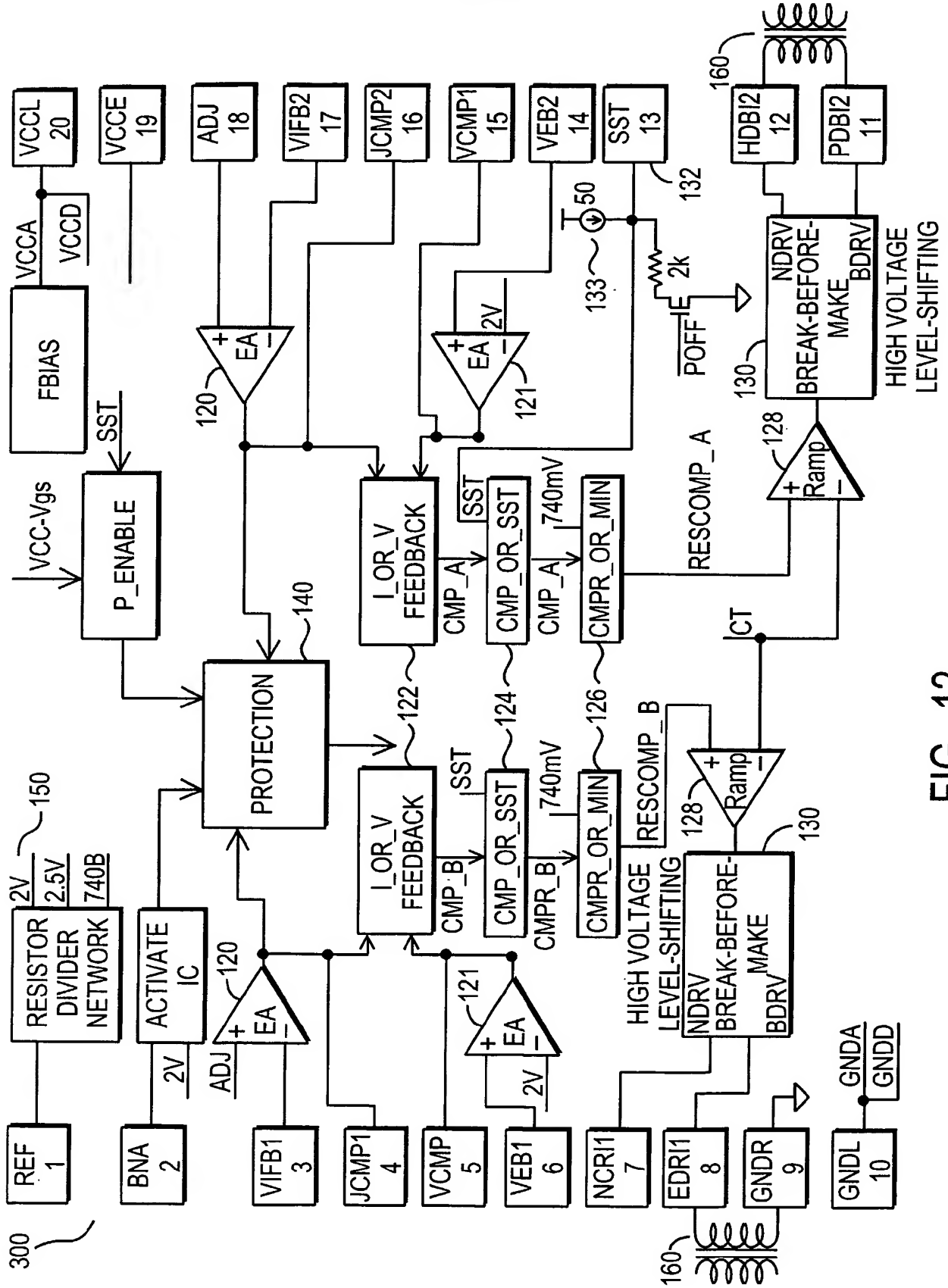

VCCL 20
VCCE 19
ADJ 18
VIFB2 17
JCMP2 16
VCMP1 15
VEB2 14
SST 13
132
HDBI2 12
PDBI2 11
160
VCCA
VCCD
FBIAS
SST
VCC-Vgs
P_ENABLE
120
EA
121
2V
50
133
2k
POFF
NDRV
BREAK-BEFORE-MAKE
BDRV
HIGH VOLTAGE LEVEL-SHIFTING
130
128
Ramp
RESCOMP_A
I_OR_V FEEDBACK
CMP_A
SST
CMP_OR_SST
740mV
CMPR_OR_MIN
CT
140
PROTECTION
122
124
126
150
2V
2.5V
740B
RESISTOR DIVIDER NETWORK
ACTIVATE IC
ADJ
CMP_B
CMPR_B
RESCOMP_B
REF 1
BNA 2
VIFB1 3
JCMP1 4
VCMP 5
VEB1 6
NCRI1 7
EDRI1 8
GNDR 9
GNDL 10
GNDA
GNDD
300

FIG. 12

FIG. 13

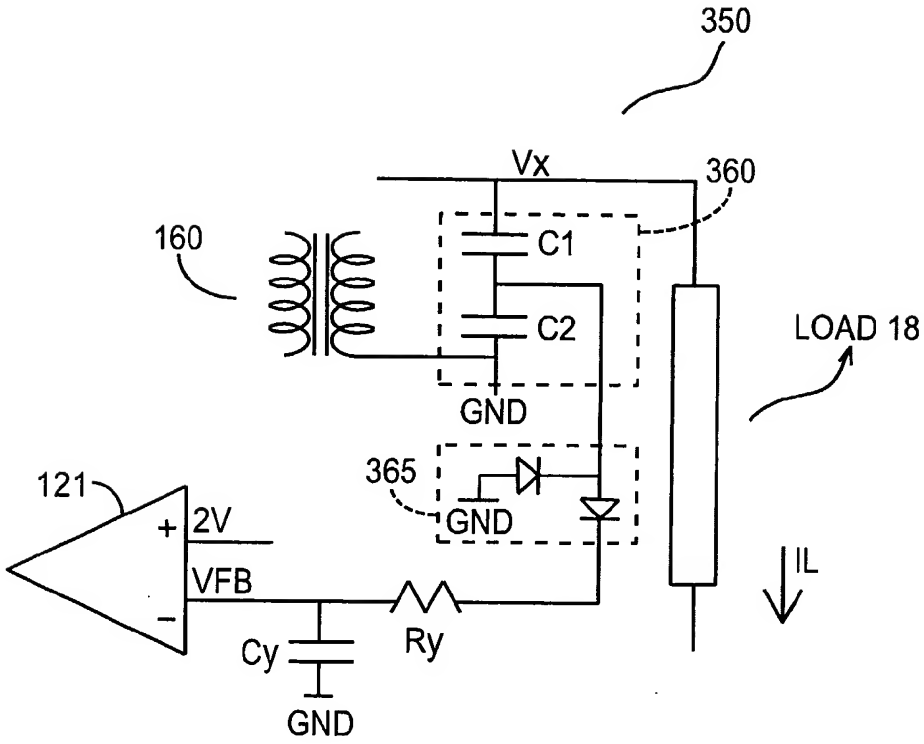


FIG. 14(a)

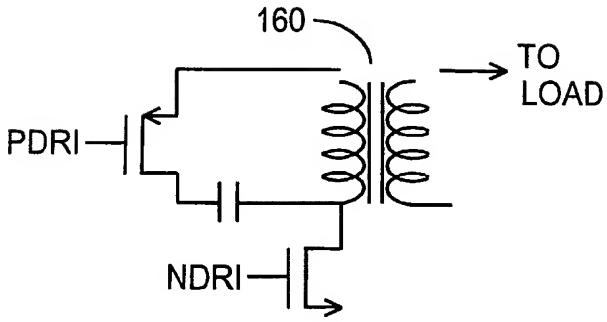


FIG. 14(b)

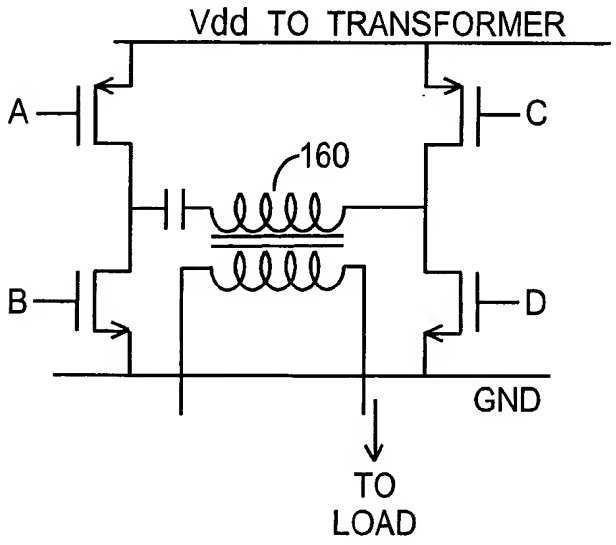
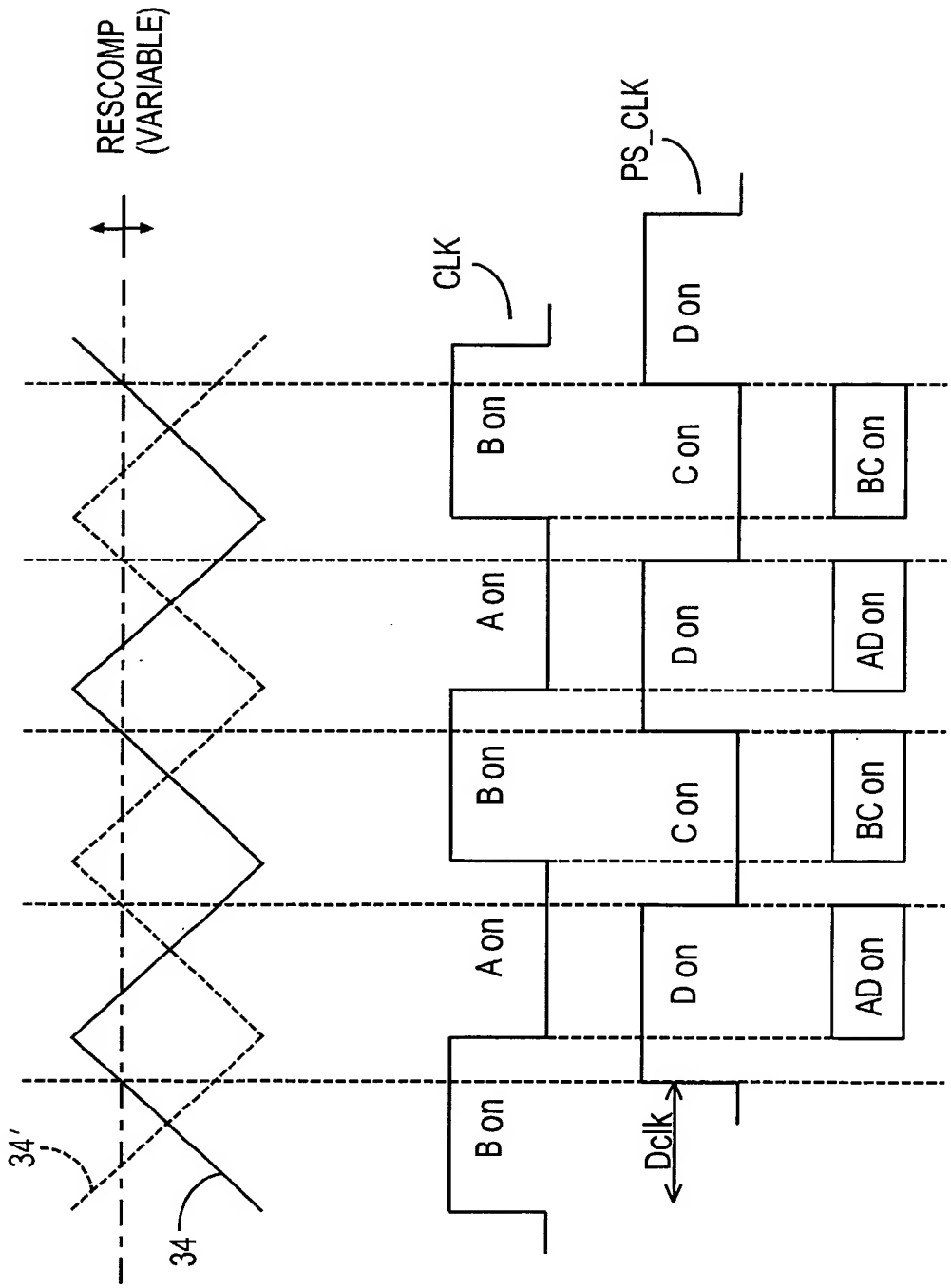


FIG. 15


RESCOMP
(VARIABLE)
34'
34
CLK
PS_CLK
B on
A on
C on
D on
BC on
AD on
Dclk

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/00129

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H05B 37/02; H02M 3/335, 3/24

US CL :Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 315/219, 209R, 224, 225, 291, 307, 308, 226, DIG.5; 363/17, 98, 25, 31, 40, 41, 95, 96, 97

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US 6,316,881 B1 (SHANNON et al) 13 November 2001 (13.11.2001), entire document.	1-56
Y,P	US 6,259,615 A (LIN) 10 JULY 2001 (10.07.2001), entire document.	1-56

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 08 APRIL 2002	Date of mailing of the international search report 07 MAY 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer CHUC TRAN Telephone No. (703) 306-5984

Deborah Perry-Leeper
Paralegal Specialist
Technology Center 2800

Form PCT/ISA/210 (second sheet) (July 1998)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/00129

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

315/219, 209R, 224, 225, 291, 307, 308, 226, DIG.5; 363/17, 98, 25, 31, 40, 41, 95, 96, 97